On improvements in metal oxide based flexible transistors through systematic evaluation of material properties

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It's the job that's never started as takes longest to finish.

- J. R. R. Tolkien

Abstract

Thin-film metal oxide (MO_x) semiconductors have opened the way to a new generation of electronics based on their unique properties. With mobilities, μ, of up to 80 $cm^2V^{-1}s^{-1}$, metal oxides do not rival crystalline silicon (μ $\sim$1000 $cm^2V^{-1}s^{-1}$) for complex applications. But such oxides do have three unique characteristics driving great interest: their mobilities persist in the amorphous form, contrary to the thousandfold drop seen in silicon; they are transparent; and they can be processed at, or near, room temperature.

Most work on MO_x semiconductors, in particular indium gallium zinc oxide (IGZO), has focused on display applications, where MO_x thin-film transistors (TFTs) are used to drive individual pixels, reducing power consumption by blocking less light than alternatives, and allowing smaller pixels due to reduced TFT sizes.

Such work has seen great advances in IGZO, but has generally not considered the thermal budget during production. By utilising the low temperature processing possible with MO_x, a new world of applications becomes possible: flexible electronics.

This work aims to improve the characteristics of TFTs based on amorphous IGZO (a-IGZO) through detailed study of the thin-film structure in relation to functional performance, looking at the material structure of three critical layers in an a-IGZO TFT.

A study of optimisation of a dielectric layer of Al_2O_3, deposited by atomic layer deposition (ALD), is presented. This dielectric, between the a-IGZO and the gate electrode, shows a three-layer substructure in what has previously been regarded as a single homogeneous layer. A study of the insulating Al_2O_3 buffer layer below the a-IGZO compared the properties of Al_2O_3 deposited by ALD and sputtering. Sputtered material has a more complex structure than ALD, consisting of multiple sublayers that correlate with the sputtering process. The structure of the two materials is discussed, and the impact on device performance considered. A detailed systematic study of the effects of annealing of a-IGZO shows a strong dependence of the density on both time and temperature. A two mechanism model is proposed which consists of structural relaxation of the amorphous material followed by absorption of oxygen from the environment.

Finally, investigation of the influence of the buffer material on the a-IGZO, and the structure of this interface showed little difference in the growth of the a-IGZO, but did reveal some changes in the interface, while a systematic study of annealing effects on the a-IGZO-dielectric interface showed some interesting changes in this structure, both of which are likely to significantly impact the operational characteristics of TFT devices.

Declaration

The work in this thesis is based on research carried out at Department of Physics, Durham, England, and at Pragmatic Printing Ltd., Sedgefield, England. No part of this thesis has been submitted elsewhere for any other degree or qualification and it is all my own work unless referenced to the contrary in the text.

All unpatterned samples were made by the author in conjunction with the engineering team at PragmatIC Printing Ltd. (PPL) at the Centre for Process Innovation in Sedgefield, while full transistor devices were made by the PPL processing team.

XPS measurements and analysis were carried out by Kratos Analytical Ltd. on behalf of PPL. All other measurements of material properties were carried out by the author at either Durham University or the Centre for Process Innovation, Sedgefield, unless otherwise stated, and all analysis was carried out by the author. Measurement of transistor transfer characteristics was performed by the PPL test team, with the extraction of specific device parameters performed using proprietary software written in house by Pete Downs.

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I also owe a debt of gratitude to everyone I worked with at Pragmatic, particularly my supervisors Pete Downs and Dr. Feras Alkhalil, who really lead the work, providing direction but allowing freedom to explore. In addition to my supervisors, I would like to thank Dr. Richard Price and Dr. Catherine Ramsdale for setting up the KTP in the first place, and providing continued support throughout. My thanks also goes to the wider teams at PragmatIC, the engineering team, the process team, and the test team - you have been a pleasure to work with and without you this would all come to nothing.

Personally, my thanks goes to my family for their steadfast support and motivation throughout this process, and to my colleagues in room 142 who have always been there to share ideas, laughs, or just a chat. My final thanks goes to every single person I have known at Trevelyan College, particularly the MCR and the SSC past and present, for being my family away from home, and always giving me somewhere to come back to.

List of Publications

Densification of a-IGZO with low-temperature annealing for flexible electronics applications

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J. G. Troughton, P. Downs, R. Price, and D. Atkinson

List of Conferences

Summer School on nanoScience@Surfaces,

August 2016

Cambridge, UK.

International Conference on Semiconductor Technology for Ultra-Large Scale Integrated Circuits and Thin Film Transistors VI (ULSIC vs TFT 6),

May 2017

Schloss Hernstein, Austria.

5^{th} International Conference on Oxide Materials for Electronic Engineering – fabrication, properties and application,

May 2017

Lviv, Ukraine.

3^{rd} Functional Oxide Thin Films for Advanced Energy and Information Technology Conference,

July 2017

Rome, Italy.

innoLAE 2018,

January 2018

Cambridge, UK.

Contents

Chapter 1

Introduction

The world of electronics has undergone a transformation over the last 20 years as technology has moved beyond the limitations of silicon to reach a world previously only imagined in fiction, a world of invisible and flexible devices that can be integrated almost anywhere. This revolution has been made possible by the realisation of new semiconductors based on metal oxides, which are not limited to being perfectly crystalline but instead operate equally well in an amorphous form, and have band gaps wide enough to allow almost complete transmission of visible light [1, 2]. This has allowed semiconducting devices to be made on thin, flexible, plastic substrates, as the materials can be deposited at room temperature and they continue to operate well even under significant bending.

Metal oxide semiconductors, particularly those based on doped zinc oxide such as indium gallium zinc oxide (IGZO), have been heavily investigated over the last 15 years, primarily for their use in display application. This is because, with their low fabrication costs, large area uniformity, high transparency, and good electrical characteristics, metal oxides are outperforming other display driving options such as amorphous silicon (a-Si) and low temperature polycrystalline silicon (LTPS). This work, driven by display manufacturers such as Samsung and LG, has lead to impressive advances, ultimately resulting in IGZO entering commercial display production in 2012 [3].

More widely, flexible electronics is a burgeoning field, with estimates predicting a combined market value of over $60 Bn by 2020, growing to over $300 Bn by 2025 [4]. While the majority of this value is derived from display technology (particularly organic

light emitting diode (OLED) displays), a significant proportion is accessible with metal oxide technology. In particular, sensing applications such as medical sensors, food safety monitoring, and environmental testing, and communications technology such as Radio Frequency Identification (RFID) and Near Field Communication (NFC), present huge global opportunities for metal oxide based flexible electronics. Such applications leverage the unique advantages of metal oxide technology, allowing low cost, high performance electronics to be integrated into our everyday lives and enabling the interconnectivity promised by the *Internet of Things*. The focus on display applications, however, has meant less effort has gone into realising metal oxide based solutions for flexible applications, leaving space for new players in the market.

To date, the focus on developing display applications has not been matched by research work looking at optimising the full production of thin-film transistors (TFTs) with processes compatible with flexible substrates. Most optimisation routes have used high temperature processes in the post-deposition steps to achieve the functionality needed for displays. But as most flexible substrates are irreparably damaged by temperatures exceeding 300 °C, alternative routes must be sought.

In order to leverage the potential of metal oxide semiconductors in flexible applications, development work is needed on low temperature processes compatible with the plastic substrates most suited to flexible applications. PragmatIC Printing Ltd., has sought to fill this gap, developing thin-film transistors based on metal oxides on thin, flexible, plastic substrates, aiming to realise the potential of this technology across a range of applications [5, 6].

1.1 Aims of this thesis

Working with PragmatIC, this thesis aims to explore the impact of deposition and post-deposition processes compatible with plastic substrates, investigating differences and changes in material structure, and the impact these have on the functionality of devices.

The work here considers some of the challenges faced by PragmatIC, exploring three key material layers: the semiconducting a-IGZO, an insulating Al_2O_3 buffer layer on

which the a-IGZO is deposited, and an Al_2O_3 dielectric layer separating the a-IGZO from the transistor gate electrode. As well as looking at these layers in isolation and the challenges specific to each, this work also studies the interface between the a-IGZO and the other two layers, utilising advanced, non-destructive techniques to gain insight into the structuring of these interfaces without disrupting them.

Where appropriate, modifications have been suggested to conventional processes, based on the findings of this work, in order to enhance device performance, and these suggestions are highlighted at appropriate points.

While this work sets out to provide solutions to certain challenges faced by PragmatIC, it also provides more widely valuable insight into the behaviour of a-IGZO that is applicable to other metal oxide semiconductors. Ultimately this work gives answers to some challenges, but leaves others open to further investigation, offering suggestions of possible avenues of exploration when called for.

1.2 Thesis Outline

This thesis opens, in the next chapter, with a brief discussion of the physics underpinning general semiconductors behaviour, and considers why metal oxides are able to perform well in the amorphous form while traditional crystalline semiconductors, like silicon and germanium, struggle. Chapter 2 then finishes with a discussion of the basics of field-effect thin-film transistors and the electrical characteristics such devices exhibit, that gives technical definitions and context to the later discussion of results.

Chapter 3 presents a wide ranging review of current literature on a-IGZO, and wider metal oxide devices, covering the development of electrically active metal oxides, the introduction of zinc oxide based semiconductors, and the move beyond this to a-IGZO. This is followed by discussion of possible device architectures, and then consider the defects commonly seen in a-IGZO and their impact on device performance, as well as how these impacts can be mitigated. Finally, this chapter examines the implementation of metal oxide TFTs in flexible form factors and the development of circuits based on a-IGZO to date.

The fabrication of TFTs was done through sequential deposition and lithographic

patterning of layers. The techniques and processes employed for this are covered in chapter 4. This again gives the context needed for the interpretation of the results presented in this thesis. This is followed in chapter 5 by descriptions of all of the experimental methods used to examine and characterise the materials and devices.

The first investigation of this thesis is presented in chapter 6, in which atomic layer deposition (ALD) of the Al_2O_3 gate dielectric is optimised for low temperature deposition through a systematic study of time and temperature variables in the ALD process. Here the times allowed for reactant species to fill the chamber and the times allowed for clearing the chamber between steps are systematically investigated with optimised values proposed, this is followed by a short study of the impact of the sample temperature during this deposition and the effect of post-deposition annealing.

Chapter 7 presents an investigation of the Al_2O_3 buffer layer, comparing the structure of materials deposited by sputtering and by atomic layer deposition. Material properties, including layer thickness and density are reported from X-ray reflectivity (XRR) measurements, and diffrences in surface energy are examined.

A wide ranging and detailed systematic study of the effects of post deposition annealing on the semiconducting a-IGZO layer is presented in chapter 8. This study involves annealing a-IGZO samples for up to 36 hours in air at temperatures up to 300 °C, with detailed measurement of the resulting change in material density and thickness examined using XRR. A two mechanism model is proposed to explain the changing density.

The final part of this thesis, chapter 9, moves beyond examining each layer in isolation to look the interplay of a-IGZO with surrounding layers of Al_2O_3. This starts with an investigation of the differences in the a-IGZO and the interface caused by using the two different forms of Al_2O_3 buffer layer first considered in chapter 7, that is, sputtered and atomic layer deposited.

The second half of chapter 9 looks at the structure of a-IGZO with a gate dielectric Al_2O_3 deposited by ALD on top of it, and the effect that thermal annealing has on this stack. This systematic study uses a range of annealing times up to 36 hours at temperatures up to 300 °C. The cause and effects of these changes are discussed along with suggestions on how this might be harnessed.

The final chapter brings together the findings from the preceding chapters, considering

the implications for device manufacturing as well as the impact of these findings on the wider field of metal oxide devices. Where challenges have been satisfactorily resolved, the implementation of this into manufacturing is discussed, and where problems remain unresolved suggestions of avenues and techniques for further investigation in future work are suggested. [7]

Chapter 2

An outline of Semiconductor Physics

2.1 Introduction

Before considering the development and current state of technology based on amorphous indium gallium zinc oxide (a-IGZO) and other metal oxides presented in the next chapter, some discussion of the underlying science of semiconductors is helpful. This chapter provides such a discussion, looking first at the basics of semiconductor physics and how amorphous metal oxides fit within this, and then looking at the characteristic behaviour of semiconductor devices under test and operation. There are myriad published works on semiconductor theory which may be referred to for detailed coverage of the subject [8–11], but the aim here is to present the key concepts needed to understand the research that follows. In particular, many of the terms with regard to device characteristics (section 2.3) are used frequently throughout the rest of this work, and while a brief description of these terms are included where appropriate, this chapter gives a more detailed reference for these.

2.2 Physics of Semiconductors

In the most simplistic terms, a semiconductor is a material with conductivity that lies between that of a metal and an insulator. This conductivity can be modulated by external factors such as temperature, environment, the introduction of additional materials (dopants) and, most significantly here, electric field.

The conductivity of a semiconductor arises because at any finite temperature, electrons in the material may become free from their parent atom through absorption of additional energy, most commonly through lattice vibrations. These electrons, and the unoccupied state left where the electron was (known as a hole), can move under the influence of an applied electric field, which is observed as electrical conduction [8]. This process is best described by electronic band theory.

2.2.1 Band Theory

Band theory arises from the Pauli exclusion principle, which says that no two identical particles can occupy the same quantum state within a quantum system [8]. When atoms are brought together, the wavefunctions of the outermost electrons overlap. As electrons are indistinguishable fermions, the overlapping of these wavefunctions causes a small shift in the electron energies away from the normally discrete, quantised, energy levels of the individual atoms. In a system with a large number of atoms, this manifests as continuous bands of allowed energies, arising as the difference between the levels becomes negligible, with bands of forbidden energies, corresponding to the forbidden energy regions in the original isolated atoms, separating them. This is depicted in figure 2.1.

In a system with zero thermal energy, the electrons sit in the lowest possible energy configuration, known as the ground state (red in figure 2.1). The difference in energy between the top of the highest occupied band in the ground state, known as the valence band, and the bottom of the lowest next available band, known as the conduction band, is called the band gap, E_g.

At finite temperatures, some electrons gain additional energy through thermal excitation. If the energy gained is greater than the band gap then that electron is promoted to the conduction band, leaving behind a hole in the valence band, corresponding to a missing electron in the atomic structure of the parent atom (shown in blue in figure 2.1). As the electron is now free from its atom it is able to move under the influence of an external electric field.

In addition, the hole left empty by the electron can be filled by a neighbouring electron, which in turn leaves another hole to be filled. This filling of holes by electrons, leaving

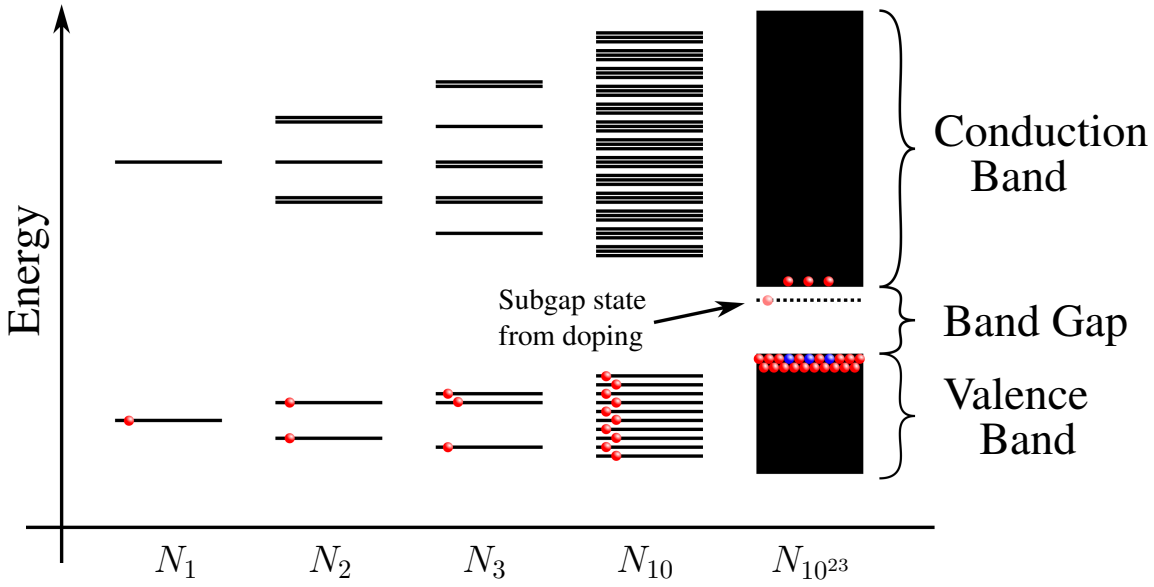


Figure 2.1: Schematic illustration of the formation of energy bands, starting with a single atom, N_1, with discrete energy levels. As additional atoms are introduced, more energy levels arise with increasingly small energy separations, until bulk materials, with the order of 10^{23} electrons, form solid bands with negligible energy separation. Red circles represent electrons filling the discrete energy levels until the band structure emerges. The blue circles represent the holes left behind in the valence band when some electrons are promoted to the conduction band. The dotted line in the band gap is a subgap state caused by doping, in this case a shallow donor state. Adapted from Krauss and Peterson [12]

behind both an energy and a charge vacancy, effectively represents the movement of a positively charged pseudoparticle. As this continues it can be seen as an additional conduction mechanism known as hole conduction. For a thorough treatment of band theory see the relevant chapter in the work from Kittel or Tanner [8, 11].

2.2.1.1 Doping

Conduction arising solely from the promotion of valence electrons to the conduction band through absorption of thermal energy is somewhat limited in most semiconductors due to the requirement for the electrons to gain enough energy to overcome the band gap. This is because the band gap in most useful semiconductors is of the order of several electron volts, but the thermal energy at room temperature is just $k_BT = 25.9$ meV. However, conduction can be greatly increased in a material by the introduction of impurities, known as doping.

Doping either provides extra electrons to the system or extra holes. If extra electrons are added, the semiconductor becomes n-type, i.e. conduction is dominated by electrons.

If additional holes are provided, the semiconductor becomes p-type, i.e. conduction is dominated by holes. In traditional covalent semiconductors this doping is used to create junctions between p-type and n-type regions, known as p-n junctions, the basis for standard diodes [11].

In the frame of band theory, the addition of dopants to a semiconductor adds additional levels within the band structure, as also indicated in figure 2.1. Specifically, additional energy levels become available within the band gap, meaning less thermal energy is required to promote an electron to the conduction band, so more electrons, or holes, are available for conduction.

2.2.1.2 The Fermi Level

One important term used in semiconductor physics is the Fermi level, E_f. The Fermi level is defined as being the highest possible electron energy within a material when that material is at 0 K, i.e. the system is in the ground state [8]. This energy is significant as it governs the likelihood of an available electron state being occupied, according to the Fermi function [11]

$$f(E) = \frac{1}{e^{(E-E_f)/k_B T} + 1} \tag{2.2.1}$$

where E is the energy state being considered, k_B is Boltzmann's constant, and T is the temperature of the system. Following this, the majority of energy states below E_f will be filled at room temperature. It is worth noting that the Fermi level in a semiconductor is halfway between the valence and conduction bands for an undoped semiconductor [8]. This does not mean electrons are found up to this point, as there are no available energy states for the electrons to exist in in this region, just that there is a finite probability that an electron could have an energy value up to the Fermi level if there was an available state.

2.2.1.3 Density of States

The number of energy states available for electrons to occupy is known as the Density of States (DoS). For ordered crystals, the density of states can be calculated from the wavefunction of the electrons combined with the the Pauli exclusion principle and the Heisenberg uncertainty principle, which is well described in van Zeghbroeck's book

[13]. However, the introduction of dopants and defects makes this significantly more challenging as the effect on the wavefunction of the material is not well known.
The effect of the DoS is to define how many electron states are available in each energy band. When this is combined with the Fermi distribution of electrons, defined by equation 2.2.1, the distribution of electrons in the semiconductor can be computed.

2.2.1.3.1 Tail States

The exact impact of defects on the DoS cannot be computed analytically, due to the unknown nature of the wavefunctions introduced. However, one consequence of defects that is worth noting is the existence of so-called tail states. These are a feature of the DoS caused by defects which induce additional energy states that extend into the ideal band gap [14]. These extended states exist continuously from either the conduction band edge or the valence band edge and extend into the band gap by an amount dependent on the defect. This causes an effective narrowing of the band gap or, if the tail states extend so far as to reach the other band, the metallisation of the semiconductor.

2.2.1.4 Carrier Transport

When an electron is in the conduction band it is free to move, and in the absence of an electric field, does so in random directions. However, when an electric field is applied, the electron moves in the opposite direction to the field due to its negative charge. The electron will travel in a straight line until it is disturbed, for example by the influence of an atom or some other scattering mechanism. The distance the electron travels is known as the mean-free path, λ, and the time for this movement is the mean-free time, τ_c.
The speed with which the electron is able to move through the material, known as the drift velocity $\boldsymbol{\nu_d}$, is directly related to the mean-free time by

$$\boldsymbol{\nu_d} = -\frac{q\mathbf{E}\tau_c}{m_e^*}, \tag{2.2.2}$$

where q is the charge on the electron, $\mathbf{E}$ is the electric field applied, and m_e^* is the effective mass of the electron.
The effective mass is an alternative mass ascribed to an electron in a semiconductor to enable the application of the free electron gas model, and results from Bragg scattering of

the charge carrier wavevectors within a crystal lattice. By modelling electrons (or holes) as classical particles with a new *effective* mass, m_e^* (m_h^*), classical Newtonian mechanics can be used to describe its motion. This effective mass is governed by curvature of the local band structure in which the electron is found, expressed as

$$m^* = \frac{\hbar^2}{\partial E^2 / \partial \boldsymbol{k}^2} \tag{2.2.3}$$

where $\hbar$ is the reduced Plank's constant, E is the local band energy, and k is the wavevector of the electron. This implies that the effective mass of a carrier is directly related to the curvature of the band energy with respect to the wavevector in the local environment. At the top of the valence band and bottom of the conduction band this is approximately parabolic and treated as such for calculations, allowing simple treatment of the effective mass of carriers. For a more complete consideration of effective mass see the books from Ferry or Kittel [8, 10]. The ratio of $\boldsymbol{\nu_d}$ to the electric field, **E**, is known as the electron mobility, μ_e, and is one of the most important characteristic of a semiconductor, given as

$$\mu_e = \frac{\boldsymbol{\nu_d}}{E} = \frac{q\tau_c}{m_e^*}. \tag{2.2.4}$$

The same argument can be applied to holes moving in the semiconductor giving the hole mobility as

$$\mu_h = \frac{\boldsymbol{\nu_d}}{E} = \frac{q\tau_c}{m_h^*}. \tag{2.2.5}$$

In a traditional, crystalline, semiconductor such as silicon, the effective masses of electrons and holes can be calculated analytically as the structure of the band is well defined. In these systems it is generally found that the curvature of the conduction band (where electrons move) is significantly greater than that of the valence band (where holes move), meaning μ_e is significantly greater than μ_h. In addition, while it is not possible to analytically assess the values in amorphous semiconductors, the same relation between μ_e and μ_h is generally found to hold experimentally.

The equations for μ_e and μ_h above make clear the importance of τ_c in determining the semiconductor properties. The main factors that affect τ_c in crystals are scattering from impurities and scattering from the crystal lattice, meaning that, in order to maximise the carrier mobility, impurities should be minimised and the crystal lattice kept regular.

This is not, however, always possible for several reasons: Doping a material, in order to increase the number of electrons available for conduction, introduces impurities which scatter the charge carriers. Thermal energy causes lattice vibrations in the material, increasing the likelihood of lattice scattering due to the interaction of the charge carrier with an atom. Lattice scattering is also caused at grain boundaries, where two different orientations of the crystal structure meet. For a detailed consideration of transport mechanisms within semiconductors see the book by T. Pruschke [9].

2.2.1.5 Crystalline vs Amorphous Semiconductors

The discussion here has been deliberately kept open with regard to the material structure of semiconductors so as to make it applicable to both traditional, covalent semiconductors such as silicon and germanium, which work best in a highly crystalline structure, and the metal oxide semiconductors, which are the focus of this work, and which operate in an amorphous configuration or in a crystalline state. However, with regard to the carrier transport there is a significant difference that must be explored.

The movement of electrons in a crystalline material such as silicon can be visualised as travelling along the sp^3 orbitals of the atoms, which overlap in the regular crystal structure, known as sp^3 hybridisation (visualised in figure 2.2**a**) giving a relatively long mean-free path and therefore large τ_c . However, if the crystal structure is disrupted by defects, or the material is completely amorphous, this conduction pathway is broken (figure 2.2**a**) leaving electrons to hop between orbitals in a process known as tail-state hopping [15]. This dramatically reduces the mobility of the semiconductor. For example, in silicon the electron mobility in single crystal material can reach over 1000 cm^2V^{-1} s^{-1} [16], but in the amorphous state this can drop to less than 0.05 cm^2V^{-1} s^{-1} [17].

Metal oxide semiconductors, on the other hand, do not rely on the overlap of these sp^3 orbitals to provide the conduction band pathway. Instead, the large s orbitals associated with the transition metal cations overlap to provide the conduction path, (figure 2.2**b**) [2]. As the s orbitals are spherically symmetrical, this overlap is the same whether the atoms are ordered in a regular crystal structure, or completely disordered in the amorphous form. This is the source of the much improved electrical characteristics of metal oxide semiconductors compared to, for example, amorphous silicon. Indeed, in the original

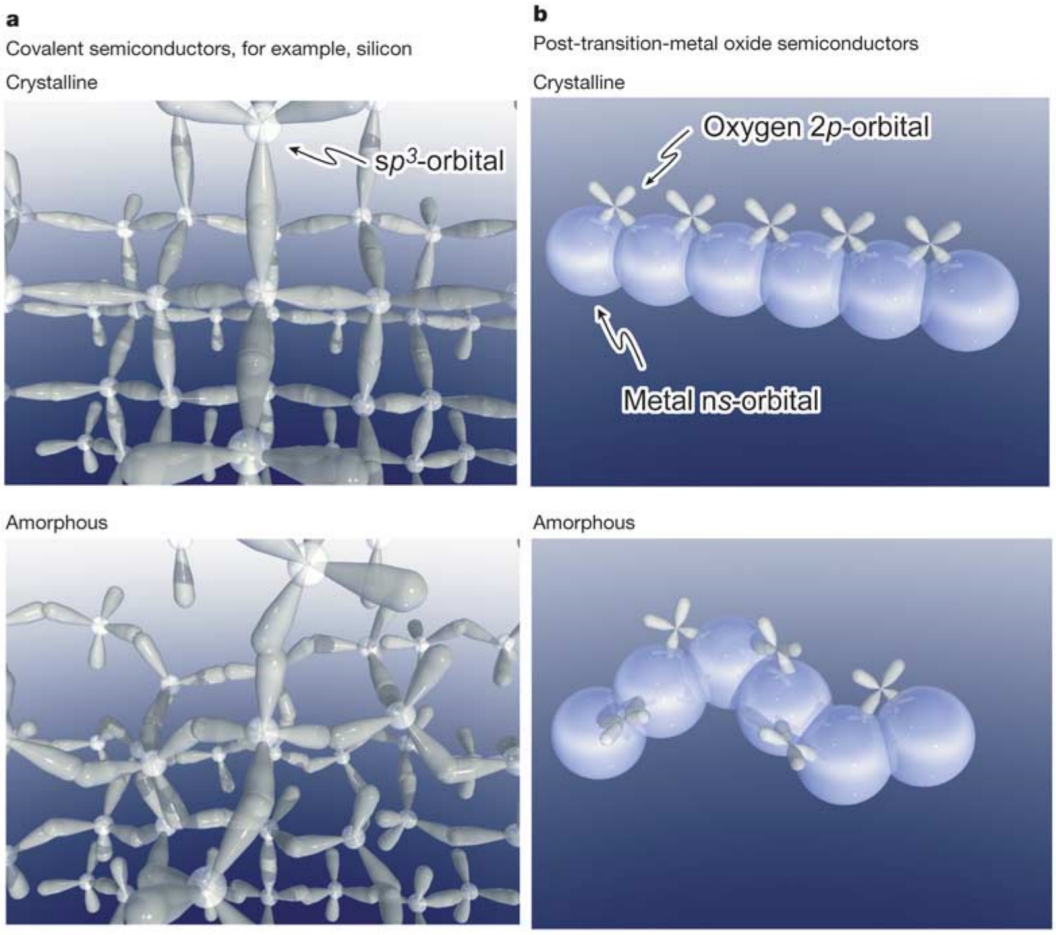


Figure 2.2: Schematic orbital drawings for the carrier transport paths (that is, conduction band bottoms) in crystalline and amorphous semiconductors. **a** Covalent semiconductors have carrier transport paths composed of strongly directive sp^3 orbitals, so structural randomness greatly degrades the magnitude of bond overlap, that is, carrier mobility. Note that the orbitals shown are illustrative, and do not show exact wavefunctions. **b** Amorphous oxide semiconductors composed of post-transition-metal cations. Spheres denote metal s orbitals. The contribution of oxygen $2p$ orbitals is small. Direct overlap between neighbouring metal s orbitals is rather large, and is not significantly affected even in an amorphous structure. Reproduced from Nomura et al. [2]

work from Nomura et al. the field effect mobility of IGZO was shown to fall by just one order of magnitude, from $\sim$80 cm^2V^{-1} s^{-1} [1] to $\sim$5.6 cm^2V^{-1} s^{-1} [2] on transition from crystalline to amorphous, and this low value of mobility has been significantly improved since, with Rim et al. demonstrating a mobility of 84.4 cm^2V^{-1} s^{-1} [18]. Further details of the difference in transport mechanisms between traditional silicon and metal oxide semiconductors can be found in the review of the subject from Kamiya et al. [15].

2.3 Semiconductor Devices

The second half of this chapter is concerned with the use of semiconductors in transistor devices. As with semiconductor theory, there are many excellent books available on transistor operation and design [19–21], so here a brief overview of the relevant terminology is presented.

A transistor, in the simplest terms, is a device capable of modulating the flow of current dependent on some external controlling influence. In this work, thin-film field effect transistors (TFTs) are considered, in which the flow of current is modulated by the application of an electric field across the semiconductor, creating a conducting channel between the contact electrodes.

The application of an electric field and its effect on a semiconductor device is known as the *field effect*. The *field effect* relies on the delocalisation of the conduction electrons, so that when a positive field is applied, electrons are attracted towards the gate, accumulating at the interface between the semiconductor and the gate dielectric. As the density of electrons at this interface increases, a conductive channel forms between the contact electrodes allowing charge flow in the device.

Figure 2.3 shows the typical behaviour of an n-type TFT. This is known as a transfer or I-V curve as it shows the dependence of the current flowing between the contact electrodes, I, on the gate voltage, V_G. In the ideal case, the TFT will have no current flow for gate voltages below 0 V and very large flow for $V_G > 0$ V, with a sharp switch between these states.

There are many different designs for TFTs, covered in detail in section 3.3.2.3, but the basic principle is the same: two electrodes contact the semiconductor on either side, and

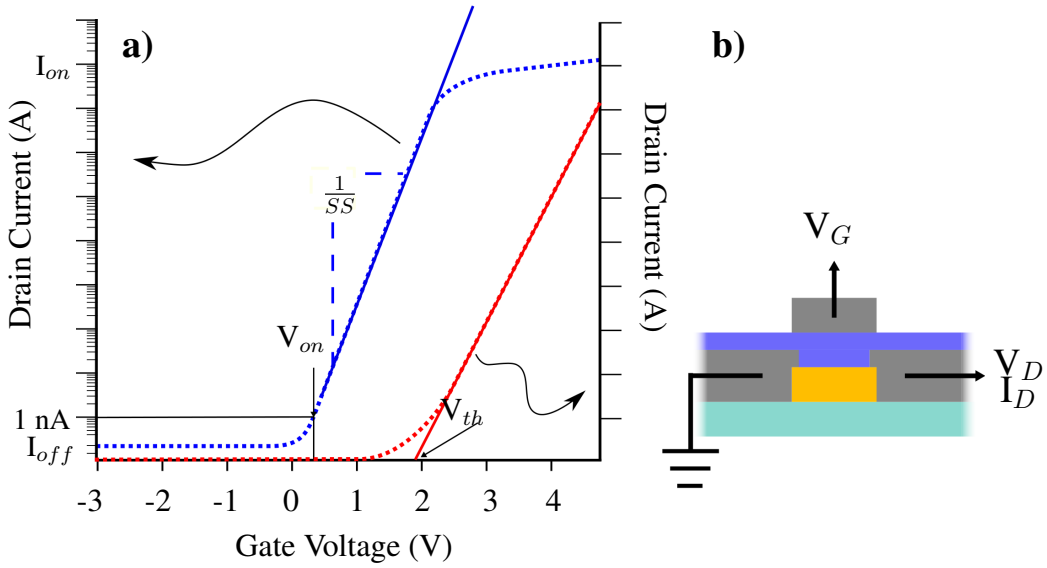


Figure 2.3: **a)** Typical transfer curve for a metal oxide TFT, showing the subthreshold swing, V_{on}, V_{th}, I_{on}, and I_{off}. **b)** shows a schematic of a simplistic TFT device.

a gate electrode is placed across the length of the semiconductor, separated from it by an insulating layer. The contact electrodes provide the source of current, while a voltage applied to the the gate electrode provides the field effect.

Marked on figure 2.3 are several key parameters that can be extracted from the transfer curve. The theoretical basis for these is summarised here, while details of how these are calculated is included in chapter 5. For a more detailed overview of this see further references [21–23]

2.3.1 Current Flow and Mobility

The current flow, I_{DS}, in the TFT is one of the dominant features of the transfer curve and is described as [15]

$$I_{DS} = \frac{W}{L}\mu C_G \left[(V_G - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right], \tag{2.3.6}$$

where W and L are the width and length of the semiconductor channel, C_G is the capacitance of the gate dielectric material, V_G is the gate voltage, V_{th} is the threshold voltage (marked in figure 2.3), and V_{DS} is the voltage across the contact electrodes. However, in practice the measured I_{DS} is lower than this suggests owing to defects in the channel, the gate insulator, and their interface [15]. To account for these defects, μ is

modified as

$$\mu = \frac{N_G - N_{trap}}{N_G}\mu_d, \tag{2.3.7}$$

where N_G is the total carrier density created by the gate voltage which can be estimated as $N_G = C_G(V_G - V_{th})$, N_{trap} is the number of carriers trapped by defects, and μ_d is the intrinsic semiconductor drift mobility given by equation 2.2.4. This form of μ is known as the field effect mobility, μ_{FE}.

2.3.1.1 Subthreshold Swing

The subthreshold swing, SS is the second noticeable feature of the transfer curve, describing how much change in V_G is needed to switch the device from "off" to "on". This is defined as $SS = dV_G/d\log_{10} I_{DS}$ and is related to trap states in the band gap as [15]

$$SS = \ln 10 \cdot \frac{k_B T}{q}\left(1 + \frac{qD_{sg}}{C_G}\right) \tag{2.3.8}$$

where k_B is Boltzmann's constant, T is the temperature, q is the charge on an electron, and D_{sg} is the density of defect-induced states within the band gap. Evaluated at 300 K this can be written as

$$SS = 59.5\left(1 + \frac{qD_{sg}}{C_G}\right) \text{[meV decade}^{-1}\text{ at 300 K]}. \tag{2.3.9}$$

This puts a fundamental limit on how quickly a device can switch from off to on at 59.5 mV decade^{-1} for perfect devices with no trap states, and provides a measure of the level of trap states in real devices: the closer SS of a device is to 59.5 mV decade^{-1} the lower the level of trap states.

2.3.1.2 Turn-on Voltage and Threshold Voltage

The turn-on voltage, V_{on}, and the threshold voltage, V_{th}, are similar but subtly different measures of when a TFT turns on. The threshold voltage is defined as the voltage at which a complete conduction channel is induced by the field effect in a device. V_{th} is measured by extrapolating the linear region of the transfer curve to the zero current point [24], as shown in figure 2.3, and discussed in section 5.4.

The turn-on voltage, on the other hand, is defined as the value of V_G when the current

flow rises above a set threshold, and is intended purely as a measure for circuit design purposes.

2.3.1.3 Leakage Current and Switching Ratio

The leakage current, I_{off}, is the current flow in the TFT when the voltage applied to the gate is less than the turn-on voltage, V_{on}. In the ideal case, I_{off} is zero and there is no current flow at all. However, due to the presence of defects in the device, some small current flow is inevitable. The value of such a current is a function both of the density of defects which give rise to it and device geometry, therefore any comparison between devices must recognise this and normalised values (with regard to μ_{FE} for example) should be used. I_{off} is particularly important in low power applications as it defines how much power is consumed when a device is inactive, and a large I_{off} can significantly increase power requirements.

Closely tied to I_{off}, and device mobility, is the on/off ratio, $I_{on/off}$. This is the ratio of the current flow in a device during the "off" phase (when $V_G < V_{on}$) and the "on" phase ($V_G > V_{th}$) in the transfer characteristics [25]. $I_{on/off}$ gives a measure of the efficiency of a transistor device. As with I_{off}, $I_{on/off}$ is strongly geometry dependent, so optimisation of device geometry is necessary depending on TFT application. Reduced channel length/increased channel width increases both I_{on} and I_{off}, so it is advantageous for high power applications where the TFT is required to pass large amounts of current, but less suitable to low power applications where increased power consumption is a limitation. For most digital circuits a value of $I_{on/off} > 10^6$ is required [24], although this can be reduced to $I_{on/off} > 10^4$ for analogue applications such as sensing [25].

2.3.1.4 Hysteresis and Device Stability

The final aspect considered here is hysteresis in the transfer characteristics, and device stability. These are considered together as they are closely related in terms of their origin, being due to trapping defects in the semiconductor-gate dielectric interface [15, 26, 27]. Hysteresis here is the reversible change in the transfer curve between positive voltage sweeps, measuring from negative to positive gate voltage, and negative sweeps, measuring

from positive to negative [28]. This most commonly manifests in metal oxide TFTs as a lateral shift in the curve without any change in its shape, and is measured as the difference in V_{th} in forward and reverse transfer curves [26, 29].

Device stability refers to irreversible change in device performance over time. This is again most commonly seen as a parallel shift in the transfer curve, and may be caused by repeated switching of the device, prolonged application of a positive or negative gate voltage (referred to as bias testing), or simply degradation with time in storage [30, 31].

The mechanisms causing such changes in device behaviour, and the connection between these two phenomena, are discussed in detail in the section of chapter 3 concerned with device defects, particularly interface electron trap sites [32, 33].

2.4 Conclusion

This chapter has provided a very brief overview of the fundamental physics underpinning semiconductors, introducing the concepts of band theory, semiconductor doping, and electronic states, along with discussion of the difference in carrier transport between traditional covalent semiconductors, such as silicon and germanium, which are only able operate effectively in highly crystalline forms, and metal oxide semiconductors, such as IGZO, which are able to operate in both the amorphous and crystalline forms. This later point is re-examined in section 3.5.3, and is one reason why a-IGZO has become a popular choice in the development of next generation electronics. Following the discussion of fundamental semiconductor physics, this chapter then discussed the parameters associated with thin-film transistor operation, considering mobility, μ, within a device, subthreshold swing, SS, various measures of current and voltage pertaining to device operation (V_{th}, V_{on}, I_{off}, and $I_{on/off}$), and changes in device characteristics with operation.

This chapter does not aim to present a thorough coverage of these topics, but is instead intended to provide a basis from which the following work can be understood. This is particularly relevant to the following chapter, chapter 3, in which many aspects of the history, development, and current state of metal oxide TFTs are reviewed.

Chapter 3

Development and present status of a-IGZO and metal oxide devices

3.1 Introduction

Understanding the wider field of metal oxide devices provides important context for this work. Therefore, this chapter reviews published literature relating to IGZO thin film transistors (TFTs), and associated materials. This starts with the applications of transparent conductive oxides (TCOs), followed by the development of metal oxide thin-film transistors (TFTs), and finishes with a survey of current applications of IGZO devices including display and flexible applications. This review is intended to summarise these fields, all of which contribute to the work later in this thesis (particularly informing choices of materials, processes, and device structures), although some of these areas are only briefly covered here. Where appropriate, suitable review articles are recommended for particular topics, of which there are many owing to the rapidly developing nature of this technology.

3.2 Transparent Metal Oxides

Optically transparent metal oxides have a variety of applications in electronics and beyond. Here, an overview of the different applications within electronics is presented, with particular focus on transparent and flexible applications, while semiconducting

applications are deferred to the following section.

3.2.1 Transparent Metal Oxides as Dielectric Materials

One of the most wide spread uses of metal oxides in electronics is as a dielectric material, particularly as the gate dielectric in transistors.

As the size of silicon transistors has reduced, due to commercial pressure to produce ever higher functionality at lower costs, the thickness of the dielectric (traditionally SiO_2) has reduced in line with other dimensions [34]. However, as the thickness of the SiO_2 continues to reduce, gate leakage (the current flow due to direct tunnelling of electrons through the film) has become a limiting factor, such that by the early 2000's, with SiO_2 thicknesses less than 1.4 nm, the leakage current could reach 1 A cm^{-2} at 1 V [35, 36].

This scaling problem has led to the hunt for materials with higher dielectric constants, κ, to replace SiO_2. These high-κ dielectrics took many forms, most commonly metal oxides such as Ta_2O_3 [37], $SrTiO_3$ [38], Al_2O_3 [34], and many others [39–50] (see figure 3.1). As highlighted in figure 3.1, the dielectric constant is inversely proportional to the band gap of these materials, so a balance has to be sought between a high κ and a large band gap, necessary to ensure good insulating behaviour. One further factor to note is that, in addition to providing good electrical isolation between the gate electrode and semiconductor, the large band gap of these high-κ dielectrics means they do not absorb light in the visible spectrum, making them optically transparent and therefore a suitable choice for transparent electronics [51]. For a comprehensive review of the requirements, potential materials, and developments in high-κ dielectrics see the review articles by Wilk et al. [34] and Wang et al. [51].

Due to its large band gap (~ 8 eV) and reasonable dielectric constant (~ 9) Al_2O_3 has become one of the most common choices for gate dielectric material [51]. Al_2O_3 is also advantageous due to the wide range of deposition techniques that can be used and high uniformity of important characteristics such as dielectric constant and refractive index, particularly in the amorphous phase [52–58]. For current device applications, Al_2O_3 is a good choice for a dielectric. However, with a lower value of κ than many other metal oxides, recent work has sought to create stacked dielectrics incorporating other, high-κ, materials into the stack, in order to further enhance device performance [54, 59].

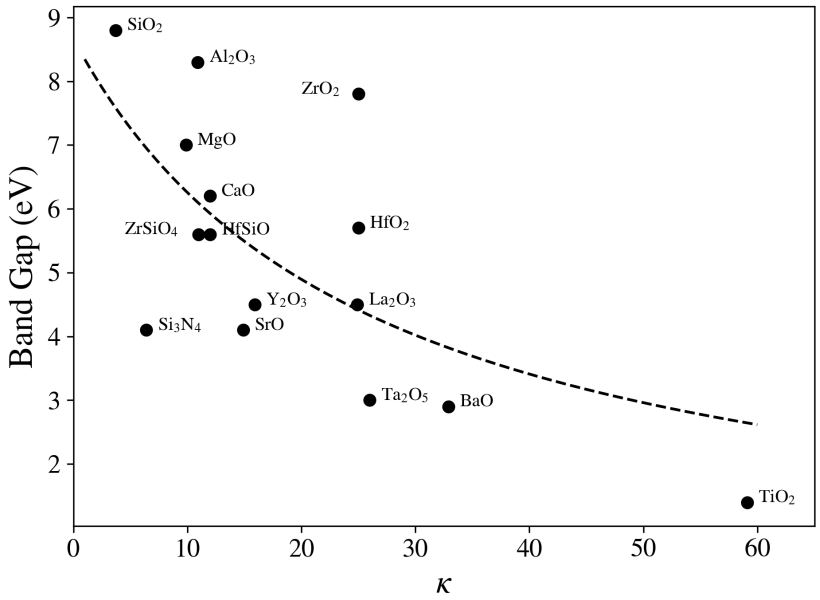


Figure 3.1: Static dielectric constant against band gap for some metal oxides, adapted from Robertson et al. [35]. The dielectric constant is approximately inversely proportional to the band gap, as represented by the dashed trend line.

3.2.2 Transparent Metal Oxides as Transparent Electrodes

The other major application of transparent metal oxides in electronics is as a conductive film, known as transparent conductive oxides (TCOs), the main application of which is as electrodes, particularly for display applications.

The first report on TCO's came in 1907 with Badeker's discovery of the conductive properties if CdO, Cu_2O, and PbO [60], although development of the field was limited throughout the first half of the 20^{th} century due to the rudimentary understanding of vacuum techniques at the time. Thermal oxidation of a metal film (deposited by sputtering), shown by Badeker, was later used to produce tin oxide [61] and indium oxide [62] films, following which chemical deposition (in the form of pyrolysis) was developed for both [63–65]. The same materials were later deposited by reactive sputtering of metal films in an Ar/O_2 atmosphere, which was also used to produce iron oxide [66].

The second half of the 20^{th} century saw a proliferation of TCO use, with applications such as anti-static coatings, heat reflecting glass coatings, window heating elements, and many others [67, 68], as well as significant use in electronics.

The overwhelming majority of electronics has used indium-tin-oxide (ITO), in part because it was one of the first TCOs to be developed in a controllable mannor [69–71], and also because of the control of the film conductivity that was achieved by controlling the incorporation of Sn [72, 73]. Alongside the development of ITO, there has been work on SnO_2 and ZnO-based films, although the former has a significantly higher resistivity and the later has only recently achieved the low resistivity values of ITO [74].

The main use of TCOs within electronics has been as electrodes in optical devices, initially as the front electrode in rectifying photocells [75] and later as the gate electrode in flat panel displays (FPDs) [76–79]. ITO has also been used as both the gate electrode and source/drain electrodes in the fabrication of fully transparent TFTs [2, 80], which is further discussed in section 3.3. The physical basis for the simultaneous good 'metallic' conductivity and 'non-metallic' transparency is discussed in the review by Edwards et al. [81].

While there are advantages of using TCO electrodes, particularly in optoelectronic applications, there are also considerable limitations. One of the most apparent, and detrimental, is the resistivity of these TCOs. For all electrodes in a TFT the minimum possible resistivity (ρ) is desired, as this reduces voltage losses and signal noise. ITO and ZnO both have reported minimum resistivity of around 10^{-4} Ω cm [74], while commonly used thin metal films have resistivity in the range of 10^{-7} Ω cm$<\rho<10^{-5}$ Ω cm (for example $\rho<10^{-6}$ Ω cm for gold [82], $\rho \sim 6 \times 10^{-6}$ Ω cm for titanium [83, 84], and $\rho \sim 2 \times 10^{-6}$ Ω cm for aluminium [85] in typical thin film thicknesses at room temperature). ITO further presents cost challenges for manufacturing due to the increasing rarity of indium [67, 86, 87].

Finally, as the field of thin-film electronics moves towards flexible applications, the use of ITO is limited as it fails quickly under strain [86, 88].

The choice of electrode material, therefore, is highly dependent on the specific application, with TCO's (still predominantly ITO) being suitable for established FPD manufacturing. New alternatives such as carbon nano-tubes, graphene, and metallic grids stand to replace ITO when optical transparency is still required but cost and/or flexibility become concerns [67, 86, 89–92], while simple metal films (or bi- and tri-layer stacks of metals) can be used where transparency is unnecessary and material and processing costs

dominate [93–95].

3.3 Transparent Metal Oxides in Metal Oxide Thin-Film Transistors

The history of thin-film transistors (TFTs) actually pre-dates the now ubiquitous silicon transistor technology, at least in a theoretical sense. The first TFT designs were patented by Lilienfeld [96–98] and Heil [99] in the early 1930's , but due to the lack of understanding of either semiconductors or vacuum technology, these were purely concept patents with no evidence of functionality. While these early designs where just concepts, they are actually very similar to modern designs, with Lilienfeld's first patent, granted in 1930, describing a metal-semiconductor field-effect transistor (MESFET) and another, in 1933, describing a metal-oxide-semiconductor field-effect transistor (MOSFET) of almost exactly the type seen today. It was not until the '60s, with significant advances in vacuum technology, that the first practical demonstration of TFTs was achieved by Weimer using polycrystalline cadmium sulphide (CdS) semiconductor with gold electrodes and a silicon monoxide (SiO) insulator [100, 101].

Around the same time as Weimer was working on CdS TFTs at RCA Laboratories, Klasen and Keolmans developed a new back-side exposure process for photolithography of the transparent, semiconducting, SnO_2 to create a self-aligned TFT structure [80]. Although there are few details of the device performance, this is the first reported instance of not only an oxide being used as the semiconductor in a TFT, but also of transparent transistors and electronics in general. Further demonstrations of metal oxide based TFTs were made by Boesen and Jocobs in 1968 [102] with lithium doped zinc oxide (ZnO:Li), and by Aoki and Sasakura in 1970 [103] with SnO_2, although both showed poor electrical performance, with low drain currents (I_D) showing no saturation. Work continued sporadically on metal oxide transistor devices with reports on antimony doped SnO_2 [104] and In_2O_3 [105]. The focus of this work was not on device performance, but rather on hysteresis effects for memory applications, so little electrical characterisation is included. It was not until 2003, with the work of Hoffman et al. on ZnO [106], that good electrical performance was shown for a metal oxide based TFT.

3.3.1 Development beyond ZnO TFTs

The work from Hoffman et al., along with concurrent work from Carcia et al. and Masuda et al. [107, 108] marked the start of a revolution in metal oxide semiconductors, and transparent electronics.

ZnO had been known as a semiconducting oxide since the early '50s [109], but until the work of these groups, commercial application was limited to passive devices such as transparent conducting films, sensors, photocatalysts, and varistors [110]. The good performance achieved by Hoffman and Masuda, even on a par with hydrogenated amorphous silicon (a-Si:H) and organic TFTs at the time, in terms of carrier mobility (at $\mu \leq 2.5$ cm^2 V^{-1} s^{-1}), came at the the cost of high processing temperatures, with devices exposed to process temperatures up to 600 °C. However, Carcia showed that similar performance could also be achieved by depositing the ZnO using radio frequency sputtering at room temperature. Following this initial work on ZnO devices, many improvements in performance and variations in fabrication methods were reported [111–114], as well as work exploring SnO_2 and In_2O_3 film and ZnO nanowires [115–119]. These advances lead to demonstrations of ZnO replacing a-Si:H in flat panel displays (FPDs) for both active-matrix LCDs [120, 121] and AM-OLEDs [122, 123].

While devices based on binary semiconducting oxides (ZnO, SnO_2, In_2O_3 etc.) showed good performance, there were still limitations, particularly with regard to control of threshold voltage (V_{th}), device stability, and uniformity. These problems are attributed to the high defect concentration within the oxide leading to an excess of free electrons, and the presence of grain boundaries in the polycrystalline binary oxide materials [15]. Some control of V_{th} has been achieved by Lim et al. through doping the deposited ZnO with nitrogen during deposition [124, 125], however, the creation of grain-boundary free ZnO over large areas, either single crystal or amorphous, remains very challenging, resulting in variations in device performance across the polycrystalline ZnO devices.

In an effort to mitigate these issues more complex oxides were proposed by Nomura et al. in 2003, particularly $InGaO_3(ZnO)_5$ (IGZO) [1]. Initially single crystal IGZO (sc-IGZO) was produced that removed issues linked to grain boundaries and greatly reducing the

density of defects such that normally-off TFTs (where there is no current flow at 0 V gate bias) were produced [1]. These devices showed excellent characteristics, with high mobility μ=80 cm^2 V^{-1} s^{-1}, V$_{th}$=-3 V, and an on-off current ratio of 10^6. It was not, however, until the following year with work from the same group showing similar results using amorphous IGZO (a-IGZO) [2], that IGZO became widely acknowledged as the leading material for next generation thin-film semiconductors. This work was particularly significant as it showed that good device characteristics, i.e. μ_e $\approx$8.3 cm^2 V^{-1} s^{-1}, V$_{th}$=1.6V, and on-off ratio $\approx 10^3$, could be achieved with processing at room temperature, enabling compatibility with the process constraints of flexible substrates. Additionally, it showed that the amorphous phase, which is stable up to around 500 °C in IGZO [126, 127], was able to perform nearly as well as the single crystal phase while being significantly easier to produce. The origin of this significant insensitivity to material structure is discussed in section 2.2.1.5 of the next chapter. This work from Nomura sparked a rush of publications on multicomponent oxides as the semiconductor for TFTs. These works looked at IGZO and many other combinations of cations with electron configuration (n-1)d^{10}ns^0 (n$\geq$4) [128], including tin-doped ZnO (ZTO) [129–133], In-Zn-oxide (IZO) [134–137], hafnium indium zinc oxide (HIZO) [138–140]. For further reviews of the development of the general field of metal oxide TFTs see the papers by Kamiya et al., Fortunato et al., Park et al., and Petti et al. [15, 25, 26, 141].

3.3.2 The growth of IGZO TFTs

Since the demonstration of IGZO by Nomura, many groups have helped develop the current understanding of the material, both through empirical study of devices, and through computational studies using molecular dynamics and density functional theory. The remainder of this section now looks at the development of IGZO devices and the understanding of various issues surrounding device fabrication. While this section focuses primarily on IGZO, much of the discussion is directly applicable to other metal oxide devices.

3.3.2.1 IGZO Atomic Composition

One area of interest for the development of IGZO has been the ionic composition of the material. The single crystal devices originally produced by Nomura, with the stoichiometry $InGaO_3(ZnO)_5$, were grown by reactive solid-phase epitaxy on an yttria-stabilized zirconia substrate [1, 142, 143]. The a-IGZO demonstrated by the same group was deposited by pulsed laser deposition (PLD) from a polycrystalline $InGaZnO_4$ target in an oxygen atmosphere and had a cation ratio, measured by X-ray fluorescence spectroscopy, of In:Ga:Zn=1.1:1.1:0.9 (in atomic ratio) [2]. Systematic studies of the effect of material composition were carried out by Hosono [144, 145], Iwasaki et al. [146], and Barquinha et al. [147]. Hosono evaluated the electron mobilities and concentration through Hall effect measurements for various film compositions deposited on glass by PLD under oxygen partial pressure P_{O_2} = 1 Pa, and also the crystalline nature of the same materials. See figure 3.2 for tertiary composition maps of the amorphous formation regions, and the electron mobilities and concentrations evaluated from the Hall effect. It can be seen that the crystalline tendency of ZnO and In_2O_3 is disrupted by mixing either with each other or with Ga_2O_3. In the case of the $(ZnO)_x(In_2O_3)_{1-x}$ combination, this is attributed to the mismatch between the wurzite structure of the ZnO and the bixbyite structure of the In_2O_3, as well as the difference in the oxygen coordination numbers [148]. The inclusion of Ga_2O_3 with ZnO or In_2O_3 (or both), further disrupts the formation of the crystalline phase, again due to a difference in oxygen coordination numbers and the tendency of pure Ga_2O_3 to exist in the amorphous phase. It was also shown that the Hall mobility of the system is relatively insensitive to composition, but that the inclusion of Ga^+ ions significantly suppresses the electron carrier concentration.

Baraquinha's work, summarised in the review by Fortunato [26] and shown in figure 3.3, looked at IGZO deposited by r.f. sputtering from a range of different composition ceramic targets, while Iwasaki used a co-sputtering system with 3 separate oxide targets. Both groups showed similar trends with regard to electron mobility, agreeing with that shown by Hosono (albeit with the field effect mobility, μ_{FE}, quoted in figure 3.3 rather than the Hall mobility, μ_{Hall}). This also agreed with the trend for an increasingly positive turn-on voltage (V_{on}) with increasing gallium content. This later trend matches Hosono's

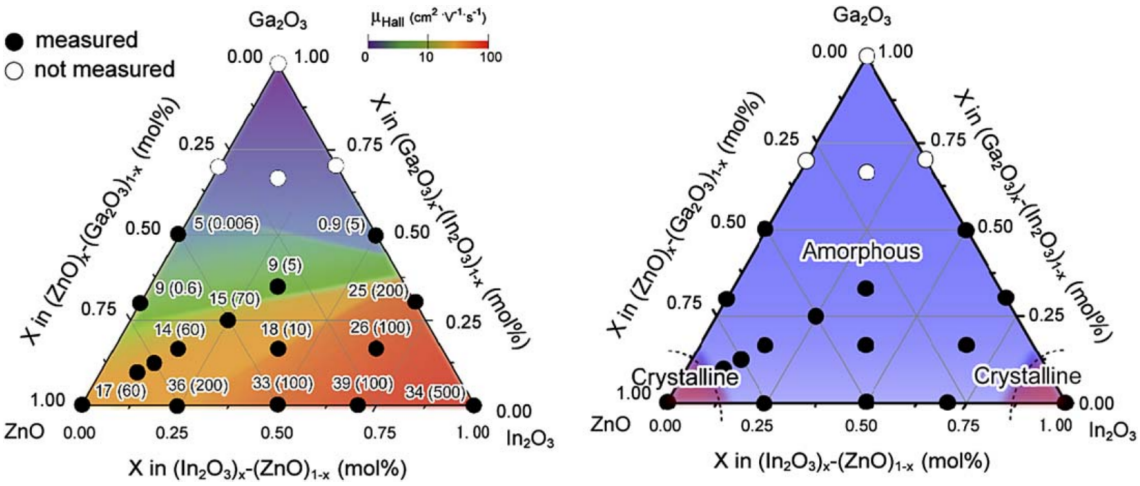


Figure 3.2: The amorphous formation region (right) and the electron mobilities and concentrations evaluated from the Hall effect for the amorphous thin films (left) in the In_2O_3–Ga_2O_3–ZnO system. Numbers in the parentheses denotes carrier electron concentration ($\times 10^{18}$ cm^3). Reproduced from Hosono et al. [144].

finding of suppression of the electron carrier concentration, forcing the fabricated devices into enhancement mode with increasing gallium content.

Given the results above many groups and commercial application projects focus solely on material with a target composition of In:Ga:Zn=1:1:1(in atomic ratio), as a balance between high mobility, a V_{on} near to 0 V and an intermediate carrier concentration, balancing the need for a reasonable carrier density in the on-state with low off-current and near zero turn on-voltage [2, 149–159].

3.3.2.2 Deposition Techniques for a-IGZO

Another area of interest to both researchers and industry is the method by which a-IGZO is deposited.

The majority of the work on a-IGZO deposition (more than 90% of published papers up to 2012 [26]) has concentrated on sputtering. The main advantage of sputtering is the availability of tools and their compatibility with existing fabrication infrastructure, along with the capacity to deposit high quality films at, or near, room temperature [25]. This continues to be the dominant method of deposition. However, in recent years, there has been a rise in alternative methods for depositing a-IGZO at lower costs and higher throughput, by eliminating the need for vacuum deposition. In most cases this has taken the form of solution processing methods such as spin coating, inkjet printing, or spray

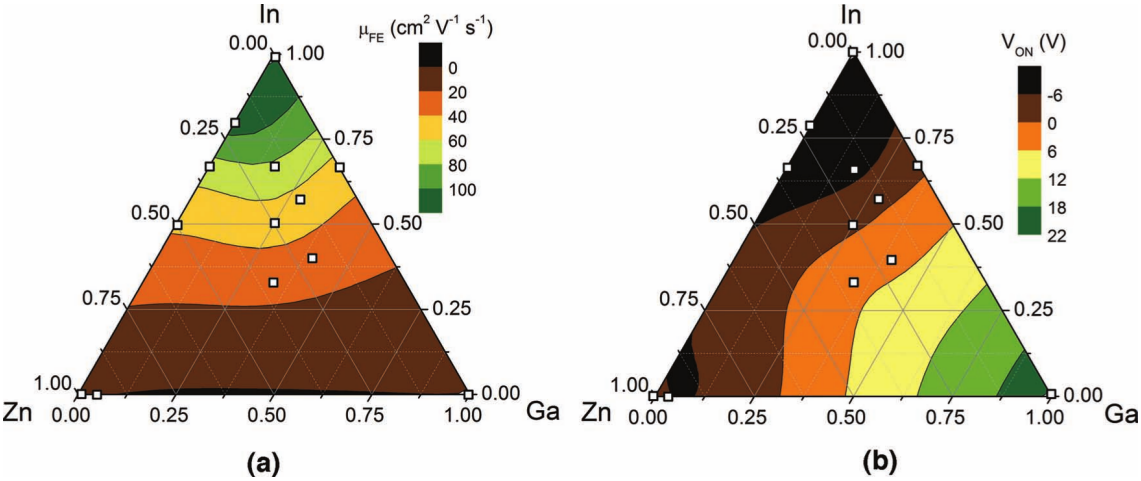


Figure 3.3: **a)** Field effect mobility, μ_{FE} and **b)** turn-on voltage, V_{on}, obtained for TFTs with different oxide semiconductor compositions, in the gallium-indium-zinc oxide system. Devices annealed at 150 °C, with $\%O_2$ = 0.4%. Reproduced from Fortunato et al. [26].

pyrolysis [160–163], although there is a growing body of work on spatial atomic layer deposition (S-ALD) starting in 2015 with work from Illiberi et al. [164] and several other research groups in the last few years [165–168].

While the possibility of atmospherically depositing IGZO is certainly an exciting one with valuable applications in large area and roll-to-roll processing, it remains very much a developing area with significant challenges, partially reviewed in the recent work from Sheng et al. [168]. For solution processing routes this is mostly in terms of the material properties, as solution processed a-IGZO has a significantly lower density than sputtered, which leads to reduced device performance in terms of mobility, threshold control, and stability (see section 3.4 for discussion of the link between density, defects, and device performance). On the other hand, the main drawbacks of the S-ALD are the cost of the equipment, which is not compatible with existing fabrication facilities aimed at a-Si:H fabrication, and the relative scarcity of precursor materials, both of which will become less problematic as this technique develops.

3.3.2.3 TFT Device Structures for a-IGZO and other Metal Oxide TFTs

There are many possible device structures which have been investigated for IGZO TFTs, the most common of which are depicted in figure 3.4. These are generally categorised by the position of the gate and source/drain contacts relative to the IGZO layer and each

other [169]. The general principle of all designs is the same - a semiconducting IGZO layer is deposited with two metallic contacts (the source and drain) in direct contact with the semiconductor, while a third transversal metallic contact (the gate) is isolated from the semiconductor by a dielectric layer [26]. This third electrode modulates the conductivity of the semiconductor by capacitive interjection of charge carriers close to the dielectric/semiconductor interface. This is known as the *field effect* and is the basis for all field effect transistors (FETs) [170].

The main device types fall under two naming conventions, firstly based on the gate position relative to the semiconductor layer (i.e. top-gate or bottom-gate). Secondly, based on the source/drain position relative to the gate and the semiconductor; if the gate and the source/drain are the same side of the semiconductor it is known as coplanar, if they are opposite sides it it known as staggered [169].

Structures optimised for Epitaxial Deposition

The first two device structures, **a)** and **b)**, in figure 3.4 are perhaps the simplest designs and were the first to be studied. These designs have two advantages: First they require very few lithographic steps (just one in the case of figure 3.4**a)**) making device production relatively cheap and quick. Secondly, the deposition of the semiconductor onto a flat, stable surface allows for epitaxial growth of single crystal material [1, 142]. The bottom-gate, top contact (BGTC) structure, alternatively referred to as staggered bottom-gate, shown in figure 3.4**a)** is particularly commonly used in research settings as commercially available Si/SiO_2 wafers can be used as the gate electrode and gate insulator respectively, meaning device structures can be created with just a single patterning step [15]. This design is, however, incompatible with commercial requirements due to the large overlap of the source/drain with the gate, causing high parasitic capacitance, which acts to reduce the switching speed of devices considerably.

Bottom-gate TFT Structures

Another disadvantage of device 3.4**a)**, common to all bottom gated designs (3.4**a)**, **c)**, and **e)**), is the exposure of the semiconducting back-channel to environmental contaminants and/or damage during source/drain definition process. The issue of the back-channel

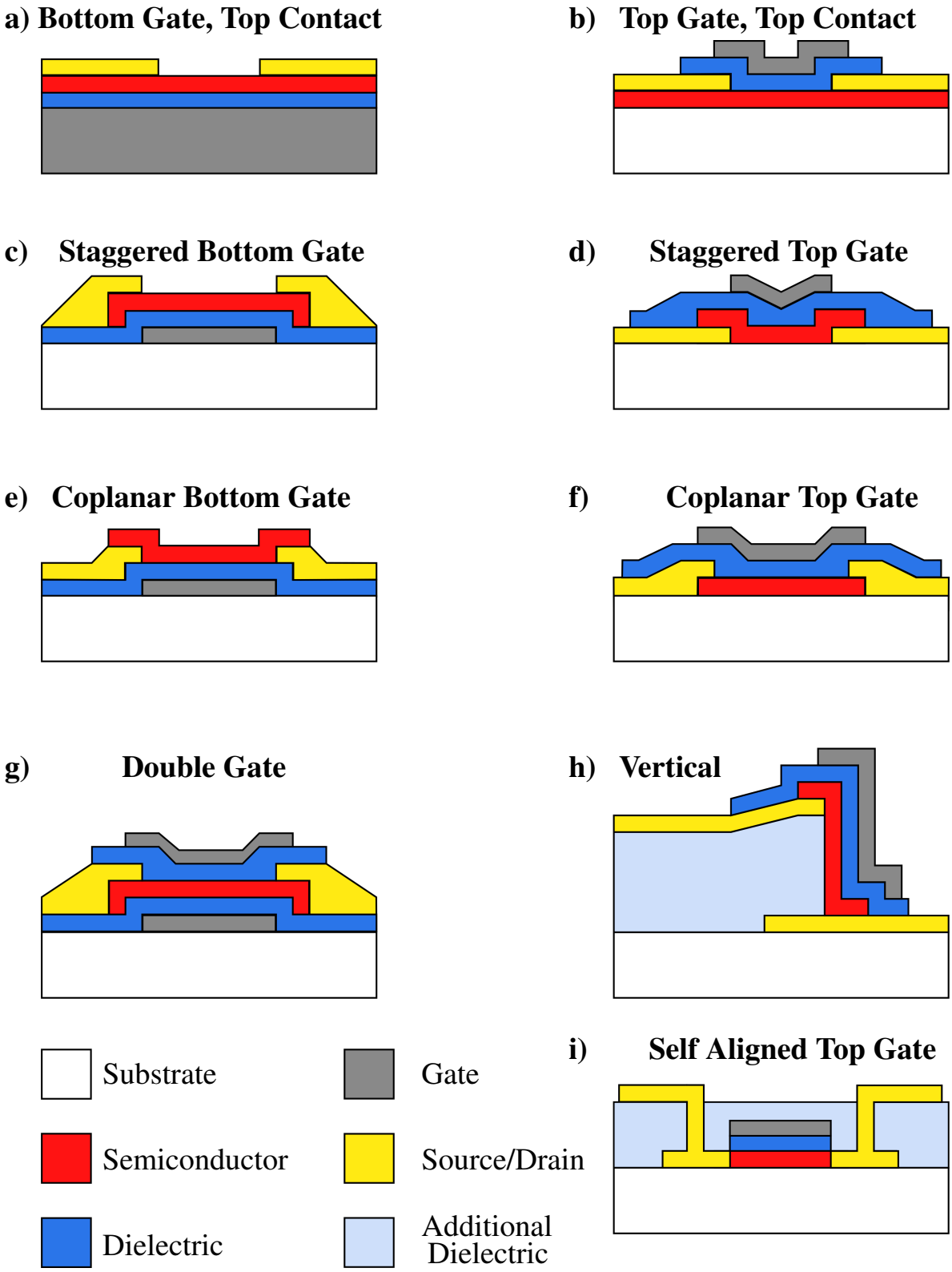


Figure 3.4: Common device architectures in literature:**a)** Bottom Gate, Top Contact with the substrate acting as the gate, **b)** Top Gate, Top Contact, **c)** Bottom Gate, Top Contact (or Inverted Staggered/Staggered Bottom Gate), **d)** Staggered Top Gate, **e)** Coplanar Bottom Gate, **f)** Coplanar Top Gate, **g)** Double Gate, **h)** Vertical, **i)** Self Aligned Coplanar Top Gate

exposure has been investigated by many groups. To prevent environmental contamination and ingress of gases, the device can be encapsulated by a passivation layer, such as SiN_x, SiO_x, Al_2O_3, various polymers, and even nano-cellulose material [138, 141, 171–177]. Devices with such a passivation layer, but which do not protect the back-channel from the effects of source/drain etching during fabrication, are known as back-channel etch (BCE) devices. In order to protect the back-channel from the effects of etching the source/drain, an extra layer, known as an etch-stopper (ES) can be introduced. This allows for more accurate etching of the source/drain electrodes [178] and enhanced device performance [141, 179, 180]. While these bottom-gated structures require additional processing steps to create stable, high performance devices, they also have some major advantages. One advantage, which has increased the speed with which IGZO devices have been integrated into commercial products, is that existing display manufacturing using a-Si:H uses a BCE design making the transfer from a-Si:H to IGZO very easy [15, 141]. In addition IGZO is particularly prone to degradation in device characteristics when exposed to light [27, 181–183], particularly UV light, as is the case when operating in display applications with a back-light (AM-LCD and some AMOLED displays for example [172]). In back-gated devices, where the gate is opaque to light the gate protects the channel region from the effects of the back-light, thereby reducing illumination bias stress effects (see section 3.4.4.3 [184, 185].

Top-gate TFT Structures

An alternative way of protecting the semiconducting material from environmental contamination is to fabricate the dielectric and gate layers on top of the device in a top-gate configuration [2, 141, 151, 186], figs 3.4**b)**, 3.4**d)**, and 3.4**f)**. This reduces the number of steps needed to fabricate devices, while maintaining protection for the channel.

Two other key advantages exist for top-gate designs: For devices exposed to light from the top, such as in typical OLED displays, the gate protects the channel from the deleterious light in the same way as discussed for the bottom-gated devices above [138, 186, 187]. Further, the use of a top-gate design allows for a self-aligned gate, defined by exposing the photoresist from the back side of the device (through

transparent substrate and IGZO layers) with the light masked by the source/drain to minimise parasitic capacitance and maximise device response speed [139, 186, 188–190]. A final advantage of top-gated designs concerns epitaxial growth as discussed above. By depositing IGZO epitaxially on an inert substrate, crystalline material can be produced in both 3.4**a)** and 3.4**b)** structures. However, structure 3.4**a)** requires a silicon substrate, making production of transparent devices impossible. Conversely, by using a top-gated design with transparent electrodes (see section 3.2.2), fully transparent devices can be produced, with reasonable performance thanks to the reduced overlap of the gate and source/drain electrodes [2, 107, 108, 131, 191].

Coplanar vs Staggered Contacts in TFTs

The second part of the device naming convention is concerned with the position of the source/drain contacts with regard to the semiconductor and the gate. Staggered structures have these contacts on the opposite side of the semiconductor to the gate, as in figure 3.4**b)**,**c)**, and **d)**. A staggered structure with a bottom gate (also known as an inverted staggered structure) is the dominant architecture of a-Si:H devices used in commercial display manufacturing, and is therefore an attractive structure for the migration of IGZO into displays in place of the a-Si:H. On the other hand, devices with contacts on the same side as the gate, known as coplanar, have other advantages, including ease of manufacturing for crystalline devices grown epitaxially [1], as well as lower contact resistance between source/drain and the IGZO [192, 193].

Double-Gated TFT Structures

As an extension to the above discussions, some research has looked at having gate electrodes both above and below the channel layer, in a so-called double-gate structure, figure 3.4**g)** [194–196]. This structure clearly requires more processing steps due to the addition of an extra gate and dielectric layer, as well as necessitating a larger device footprint to accommodate the increase in potential lithographic alignment mismatch, and a more complex driving scheme [180]. The benefit of these increased requirements are significantly improved field effect mobility, μ_{FE}, reduction of the subthreshold swing SS (Lim et al. have reported nearly a doubling of μ_{FE} and halving of SS [197]), device

stability [198], and reduced device noise [199] owing to the change in field distribution in the channel from the second gate. Despite these improvements, double-gate structures currently remain a research interest, with little promise thus far of making it into commercial devices.

Vertical TFTs

The final device structure, depicted in figure 3.4**h)**, is the vertical TFT. This design has come to attention as the push for reduced device footprint has forced researchers to consider alternatives to planar geometries [25]. Here the channel is defined by the thickness of a device layer, commonly an additional dielectric layer as in figure 3.4**h)** [166, 200–203], although the channel has also been defined by the thickness of the gate or the semiconductor itself [204–207]. This approach is currently very new and only a small amount of work has used it.

TFTs vs MOSFETs

It should be noted that, while the operation and structure of TFTs is similar in design to the more common MOSFET (metal-oxide-semiconductor FET) design in silicon technology, it does have some fundamental differences. Figure 3.5 shows schematics of a simple TFT and MOSFET showing some of these differences. One of the most significant differences is in the substrate. In the most common form of TFT, the substrate is an insulating material, normally glass or polymer, whereas MOSFETs are built on a silicon wafer which acts as both substrate and the semiconductor. As the silicon wafer is a single crystal, device performance is significantly enhanced compared to polycrystalline or amorphous material, with electron mobility 3 or 4 orders of magnitude greater, minimal device hysteresis, and excellent stability. However, this higher performance requires a much greater thermal budget, with processing temperatures often in excess of 1000 °C, compared to TFT fabrication which is possible down to room temperature [2]. A final major difference is in device operation. While both TFTs and MOSFETs make use of the field effect to modulate the conductance of the semiconducting channel, in TFTs this is done by inducing a charge carrier accumulation layer near to the dielectric/semiconductor interface, where as in MOSFETs this is achieved by creating a charge inversion region

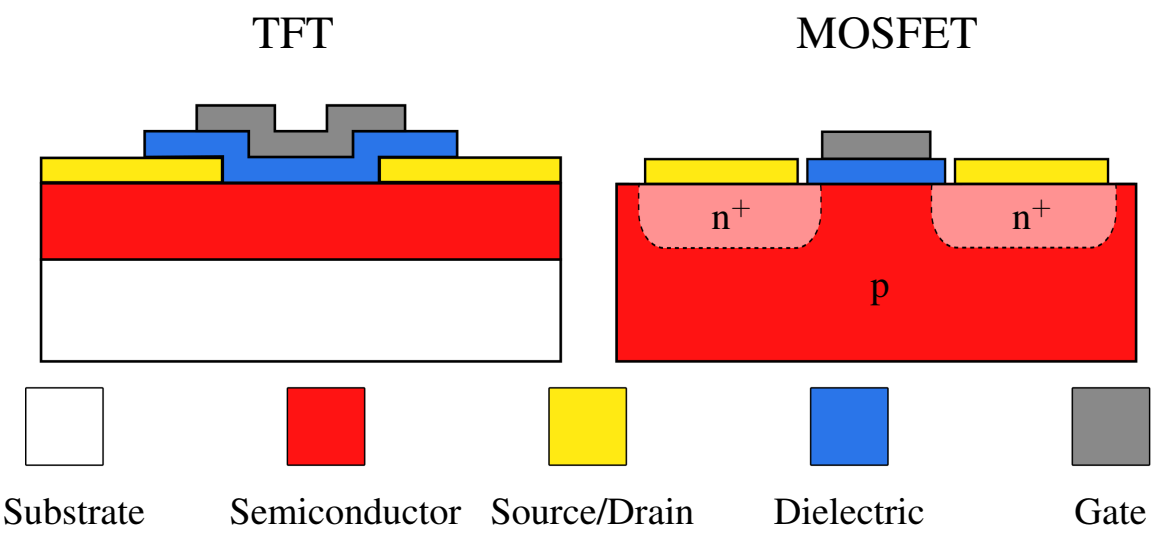


Figure 3.5: Example TFT and MOSFET designs for comparison, both using top gate, top contact designs. The light, dotted region in the MOSFET indicates the doped region, this is n-type doped if the silicon wafer is p-type, or p-type doped if the silicon is n-type.

in the same area (i.e. an n-type conductive layer in p-type silicon). This is achieved by doping regions in the silicon substrate.

3.3.2.4 Buffer Layer in TFTs

Where devices are fabricated with a top gate, particularly when using a polymer substrate for flexible applications, it is common to include a buffer layer between the substrate and the a-IGZO. This buffer layer helps create a smooth, stable platform onto which the a-IGZO is deposited, necessary as most flexible substrates have a high native roughness (most polymer substrates typically have a surface roughness of around 50 nm to 500 nm depending on the preparation conditions, much higher than, for example, typical silicon wafer roughnesses of less than 10 nm). This buffer layer also acts as a barrier to prevent ingress of moisture and gases from the polymer and/or environment [208–212]. While this buffer layer does not show any direct electrical behaviour, defects at the interface with the semiconductor can play a significant role in determining device characteristics, as described below in the discussions of defects. The inclusion and optimisation of such a buffer layer, often Al_2O_3, has been shown to significantly improve device characteristics, in particular negative bias stress (see section 3.4.4.2) [212, 213]. The properties of such buffer layers are discussed in chapters 7 and 9, where work is presented comparing Al_2O_3

buffers deposited by atomic layer deposition and sputter deposition.

3.4 Defects in a-IGZO and general Metal Oxide TFTs

Having detailed the development of amorphous metal oxide applications, and specifically that of a-IGZO TFTs, this review now turns to the focus of this work at large - the understanding and control of defects in a-IGZO TFTs. This is broken down into a discussion of the major defect types, their effect on device performance, and the different measures reported to limit or harness these effects. This discussion heavily informs the work in this thesis and defines the main motivation of this work.
Of note is that, while most defects are detrimental to device performance, some defects actually contribute to the high carrier density found in a-IGZO which makes it such a useful material. The general topic of defects in a-IGZO TFTs has recently been well described by de Jamblinne de Meux [14].

3.4.1 Defects in the Channel Region

There are three main defect types present in the channel region of an a-IGZO TFT: oxygen vacancies, metal-metal bonds, and hydrogen incorporation [141]. The effects of these on the static transfer characteristics are discussed here, while their effect on device stability is considered separately.

3.4.1.1 Oxygen Vacancies

Oxygen vacancies (V_O) are perhaps the most complex and impactful defects in the bulk channel. Vacancies can form during deposition of the a-IGZO or through removal of oxygen atoms post deposition. The amount of oxygen present in the film is related to the level of oxygen vacancies, although it is not a direct measure as oxygen can also be included in the film as interstitial, unbound species. The exact level of oxygen needed to ensure semiconducting behaviour in a-IGZO is not well characterised as the reporting of oxygen content in films is sparse (instead most works report the stoichiometry of the target and the O_2 partial pressure during deposition). However there are indications that films with as little as 60% of the stoichiometric oxygen content still show semiconducting

behaviour, albeit significantly degraded compared to the performance of material containing more oxygen [214]. In the vicinity of an oxygen vacancy several local structures can arise, as depicted in figure 3.6, each having different effects on the electrical properties of the devices, particularly the density of sub-gap states within the density of states (DOS).

Where V_O is surrounded by a small number of cations, as in **(a)**, or if the vacancy is next to a large free space void, as in **(b)**, both deep and shallow electron traps are formed [215]. These trap sites have a significant effect on the transfer characteristics of devices, as well as impacting on the operational stability (discussed separately below).

As the name suggests, these sites trap electrons (two electrons are trapped at an oxygen vacancy to create a neutral defect), reducing the carrier concentration and increasing the subthreshold swing (SS), while also contributing to hysteresis in the transfer characteristics. SS (see section 2.3.1.1) is directly related to the density of sub-gap trap sites according to [15]

$$SS = ln10 \cdot \frac{k_B T}{e}\left(1 + \frac{qD_{sg}}{C_G}\right) = 59.5\left(1 + \frac{qD_{sg}}{C_G}\right) \text{[meV decade}^{-1}\text{ at 300K]} \quad (3.4.1)$$

where k_B is Boltzmann's constant, q is the elementary electron charge, C_G is the gate dielectric capacitance and D_{sg} is the trap density, made up of trap states at the dielectric-semiconductor interface, D_{it}, and in the bulk channel, N_{sg}. As $N_{sg} \gg D_{it}$ (around 5 orders of magnitude difference has been reported [15, 216]), defects in the channel bulk are effectively responsible for the magnitude of SS. Since SS is a measure of how much voltage is required to switch the device from off to on, a lower SS is desired to reduce the device operating voltage [217]. The majority of defects that influence SS are deep within the band gap, whereas shallow trap states, around 0.1-0.3 eV below the valence band, contribute to the hysteresis in the device performance, as they trap electrons under positive gate bias, but release them again under negative gate bias. This means additional bias is needed to detrap these carriers before switching is observed [15, 32, 218].

Alternatively, where a vacancy is surrounded by many cations, particularly where these form a dense edge-sharing network, a shallow donor level is created. This shallow donor level is the main contributor to the carrier density in a-IGZO, and is therefore vital for

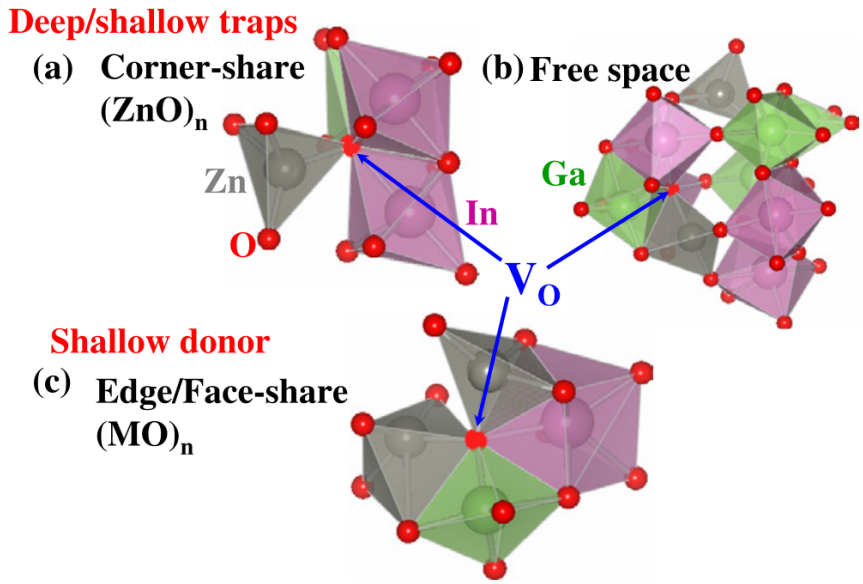


Figure 3.6: Local coordination structures of some oxygen deficiencies. The small red spheres represent O ions, green spheres are Ga, gray spheres are Zn and pink spheres are In atoms. The red spheres indicated by the arrows are oxygen vacancy sites. 'Corner-share', 'Free space' and 'Edge/Face-share' describe the structures around the oxygen vacancy sites. Reproduced from Kamiya et al. [15].

charge transport in devices [2, 214, 219].

There are several different reported methods aimed at controlling the level of oxygen vacancies in a-IGZO devices. One such approach is controlling the level of vacancies in the material during deposition. This has been demonstrated well in sputtered and pulsed laser deposited a-IGZO where the oxygen partial pressure in the reaction chamber was varied to reduce V_O, with increasing partial pressure and giving rise to a corresponding reduction in the carrier concentration [220–223].

Post deposition annealing has also been shown to reduce V_O, either by annealing in a pure O_2 atmosphere or in air [224–226], although care must be taken not to cause excess oxygen to be included in the film, as this can also lead to device degradation [126]. While most demonstrations of annealing have taken place at relatively high temperatures, it has also been shown that low temperature annealing can still contribute to a reduction of V_O [159, 177].

3.4.1.2 Metal-Metal Bonds

Associated with oxygen vacancy defects, particularly in oxygen poor-materials, is the presence of metal-metal bonds. These bonds form where there are insufficient oxygen

atoms, leaving under-coordinated metal ions to bond together to eliminate dangling bonds. These metal-metal bonds induce additional deep sub-gap states in the upper half of the band gap, below the conduction band minimum (CBM) [227, 228], with their exact position determined by the surrounding ionic environment. The ill-defined position of these states leads to a wide distribution of observed states, and ultimately to tail-states extending throughout the band gap [229]. The presence of extended tail-like states throughout the band gap can significantly increase leakage current in the off state, I_{off}.
A reduction in metal-metal bonds follows much the same lines as the reduction in V_O, as metal-metal bonds are most commonly found in oxygen poor materials, meaning the prevention of metal-metal bonds during deposition and post deposition annealing can both be utilised. However, once metal-metal bonds are formed, they are harder to eliminate than oxygen vacancies due to the energy required to break these bonds, meaning post deposition annealing requires higher energies (i.e. higher temperatures). The thermal budget of flexible substrates is relatively low (as discussed elsewhere in this chapter) so high temperatures cannot be used to produce flexible devices, and so it is preferable to deposit material under optimised conditions.

3.4.1.3 Hydrogen Incorporation

The final major defect type common in the bulk of the channel layer is the incorporation of hydrogen. This can happen through incorporation during deposition [230], with annealing under certain conditions [230–232], and via diffusion from the materials either side of the a-IGZO, namely the gate dielectric, etch stopper or passivation layer (in bottom gated devices), or the buffer layer (in some top gated devices).
There has been much debate over the role of incorporated hydrogen in a-IGZO, but a generally accepted consensus has been reached over the last couple of years [210, 233]. The effect of hydrogen is split into two parts, with each dominating at different H concentrations. At lower concentrations, suggested to be up to around 2×10^{21} cm^{-3} by Han et al. [210], hydrogen in the film either bonds to weakly bound oxygen to create -OH groups [234], or replaces oxygen at vacancy sites to passivate the vacancy [210, 235, 236]. By passivating these oxygen related defects, the hydrogen improves device performance, giving lower subFthreshold swing, hysteresis (due to reduction in defect density), and

increased carrier concentration [233, 237]. The latter effect is due to the fact that singly charged hydrogen states are stable, meaning the hydrogen acts as a shallow donor [233, 235].

At higher levels, above 2×10^{21} cm^{-3}, however, additional hydrogen no longer improves device performance. Instead, the additional hydrogen forms a conductive channel near the dielectric interface that negatively shifts the turn-on voltage by an amount proportional to the level of additional hydrogen [210]. As hydrogen is a particularly mobile species it can be hard to control the levels of hydrogen in a film.

While a consensus has started to emerge in recent years, a coherent overview of all mechanisms and potential treatments is still lacking. The field of a-IGZO (and general metal oxide TFTs) would benefit greatly from the publication of a comprehensive review of this subject.

3.4.2 Defects in the Gate Dielectric

The gate dielectric itself can also host defects that have a significant effect on device performance. Specifically, hydrogen can be incorporated into the dielectric layer. That can be Al_2O_3, as is used in this work, HfO_2, SiN_x, SiO_x, or any of the other the gate dielectrics used elsewhere, and acts as a charge trapping site [238–240]. Similarly, any oxygen vacancies or under-coordinated species in the layer can act as either deep or shallow trap sites, much as they do in SiO_2 used in traditional electronics [241,242]. These traps, for the most part, are quite shallow, so that they trap electrons during positive gate bias and release them again during negative bias. While this weak trapping means that the effect only has a small impact on long term device performance, discussed below, it does contribute significantly to the hysteresis in the transfer characteristics as the trapped electrons act to shield the a-IGZO channel from the gate bias [243].

As with elimination of oxygen vacancies and metal-metal bonds in a-IGZO, attempts to reduce the defect density in the dielectric take two approaches: optimisation of the deposited material and post-deposition annealing. By reducing the level of native defects, most commonly by optimising the process used to deposit the gate dielectric, much of the need for further processing is eliminated. However, it has been shown, particularly

where non-optimised deposition was necessary, that annealing has a significant effect on final device performance [244, 245]. This optimisation of the gate dielectric is presented in chapter 6 and the effect of annealing is studied in chapters 6 and 9.

3.4.3 Defects at the interface between the channel and the surrounding dielectrics

The final location of defects with significant impact on device performance is at the surface of the a-IGZO channel, at the interface between either the gate dielectric (the front channel) or the passivation/etch stopper/buffer layer (the back channel). Defects at these interfaces can occur for a variety of reasons, including diffusion of material at the interface (be that the deposited material or unintentionally included species such as hydrogen), native roughness of the material onto which the a-IGZO is deposited, or damage from deposition and patterning of materials after a-IGZO deposition. These defects again act as trap sites, contributing to both hysteresis, as discussed above, and device stability, discussed below.

Where bottom-gate devices are concerned, the most effective route to reduce these defects is the inclusion of an etch stopper layer, which is now common practise in most devices [178, 179, 246, 247], though care must be taken during the deposition of the etch stopper, as this may cause defects in the a-IGZO [248]. For top-gate coplanar devices, where the contacts are deposited on top of the a-IGZO and the channel then defined through lithography, the etching of the contacts can cause significant damage to the interface [249] so either an etchant that does not significantly etch a-IGZO, such as H_2O_2 should be used [196, 249], or an off-set structure can be used as the self aligned coplanar structure of figure 3.4i), and demonstated by Kim et al. in figure 3.7.

3.4.4 Device stability

The issue of device stability is treated separately here for two reasons; firstly because it is a highly significant issue with a great deal of work focusing on it, and secondly because it is impacted by almost all types of defect.

Device stability here refers to how much the static characteristics of the IV sweep (i.e.

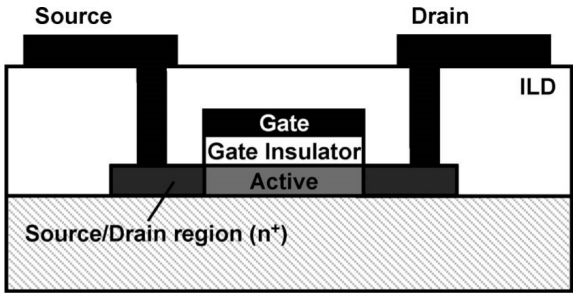


Figure 3.7: Cross-sectional structure of self-aligned top-gate a-IGZO TFTs. Reproduced from Kim et al. [139].

SS, V_{th}, I_{on}, I_{off}, μ) change during or after some form of stress. This is normally tested by holding the gate electrode at the positive (for positive bias stress, PBS) or negative (for negative bias stress, NBS) extreme of the expected functional range of the device, holding the source electrode at ground, and either applying a voltage equal to the gate voltage (for constant current measurements) to the drain electrode or holding it at ground. Biasing can then be applied for various lengths of time under multiple different environmental conditions often including light and/or temperature control.

The significance of device stability stems from the need for devices to perform consistently over extended periods of time and many thousands of cycles. In display applications, small variation in device characteristics can cause obvious and immediate variation in the display output [250], while sensing applications rely on consistent operation of comparators with fixed V_{th} to make accurate measurements, and low power circuits, such as RFID tags require "normally-off" devices with a stable $V_{th}>0$ V, so that no power is wasted and to ensure proper modulation of the carrier signal.

3.4.4.1 Positive Bias Stress

It has been shown, for almost all conditions that have been considered, that applying positive gate bias stress (PBS) causes a positive shift in the transfer curve for the devices (ΔV_{th}) but very little change in the mobility (μ) or subthreshold swing (SS) [187, 251–258], see for example figure 3.8**a)** from Lee et al. [187].

In conventional a-Si TFTs, similar testing has been carried out with two degradation mechanisms identified: defect creation in the channel and charge trapping in the dielectric or at the interface between the dielectric and the channel [259, 260]. Defect creation was

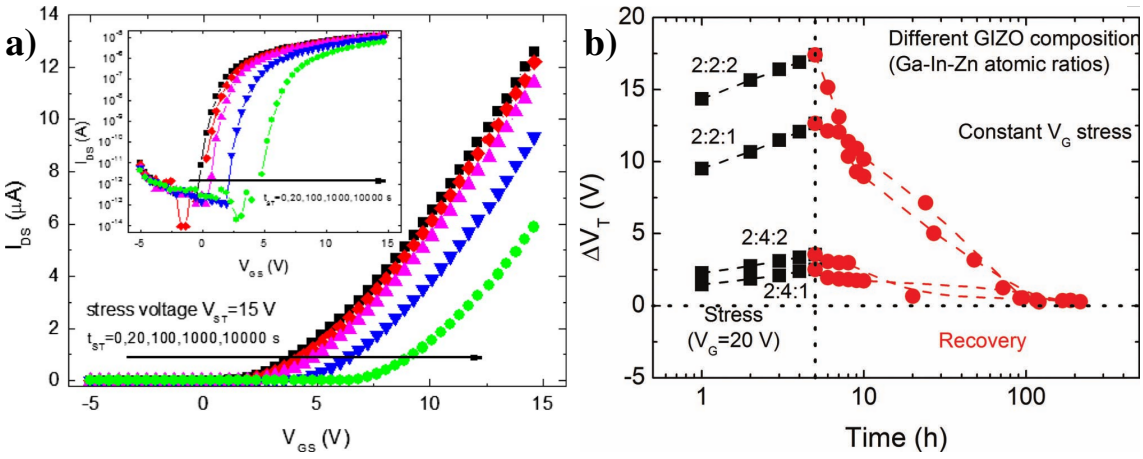


Figure 3.8: **a)** Linear transfer I_{DS}-V_{GS} curves for a-IGZO TFTs as a function of bias stress time (t_{ST}). The inset shows the bias-stress-induced shift of log(I_{DS})-V_{GS} curve. The sweep was done at V_{DS}=0.5 V in both. Reproduced from Lee et al. [187]. **b)** ΔV_T obtained on gate-bias stress measurements during 5h for oxide TFTs with different IGZO composition, annealed at 150 °C. Reproduced from Fortunato et al. [26].

shown to degrade both μ and SS, while charge trapping caused only a positive shift in ΔV_{th}. Based on this, it has been concluded that PBS in a-IGZO only causes charge trapping (with no additional defect creation) [15, 141, 180].

This charge trapping can occur at any of the trap sites discussed above, most significantly in the dielectric or at the interface between the dielectric and the a-IGZO. This process is almost identical to that which causes hysteresis between the forward and reverse transfer characteristics - i.e. trap sites capture an electron, creating a negatively charged layer which shields the a-IGZO from the positive gate bias, reducing the effective bias seen by the a-IGZO meaning V_{th} of the device increases. Unlike with hysteresis, the electrons become tightly bound and remain stable at the defect sites even under negative gate bias. However, it has been shown that recovery of the original V_{th} is possible after a relaxation period, as seen in 3.8**b)**. This recovery is hastened by elevated temperatures [15, 26], but has been shown to occur even at room temperature [254, 257].

One additional contribution to PBS occurs in bottom gated devices with exposed back channels. Here ambient water and oxygen can be adsorbed/desorbed from the surface causing additional shift in V_{th} [217, 261, 262] which can be effectively eliminated by the inclusion of a suitable passivation layer [263, 264].

3.4.4.2 Negative Bias Stress

In contrast to positive bias, negative biasing of devices shows remarkably little effect on device characteristics when carried out in the dark [15, 265, 266]. What little shift seen is similar to PBS, with no change in μ or SS, and a small ΔV_{th}<1 V, with the original characteristics recovered after an anneal. This is explained similarly to PBS, now with trapping of holes at defect sites causing a positive shielding effect and a subsequent lowering of V_{th} [180]. As a-IGZO is an intrinsic n-type semiconductor, there is a very low density of holes native to the material and so little positive charge to trap, which limits ΔV_{th}.

3.4.4.3 Illumination Bias Stress

Many applications of a-IGZO involve illumination of devices. In display applications this comes either from the back light used in LCDs or from the pixels themselves in OLED displays, while in transparent, and many non-transparent circuits this light comes from the ambient environment.

It has been shown that such illumination has a negligible effect on PBS [267], but a significant effect on the negative bias stress, known as negative bias illumination stress (NBIS).

Figure 3.9 shows a typical response to NBIS with **a)** illumination wavelength **b)** stressing time, with illumination at an energy less than the band gap and **c)** stressing time with illumination at an energy greater than the band gap. This figure shows that NBIS causes two significant changes in the transfer characteristics: enhanced negative ΔV_{th} and an increased off-current, I_{off}. It can also be seen that the effects of NBIS are dependent on the wavelength of the illuminating light as well as the time, with little response when the energy is significantly below the band gap of $\sim$3 eV, some enhancement in the negative shift near the band gap, and significant negative shift and increased I_{off} with illumination above the band gap energy. This has been explained by a hole-trapping model proposed by Lee et al. [268], in which illumination excites electrons from the valence band to subgap electron traps and the resulting holes are transported to trap sites at the dielectric-semiconductor interface.

While the model from Lee explains the enhanced negative ΔV_{th}, it does not explain the increase in I_{off}, leading Kamiya et al. to propose a slightly different model in which electrons are promoted from deep-subgap states (such as those created by some oxygen vacancies and metal-metal bonds) to the conduction band. This model explains both the shift in V_{th}, and the increased I_{off} as there is a higher concentration of charge carriers in the conduction band even in the "off" state. These models are supported by the reported dependence of ΔV_{th} on the thickness of the channel, where devices with a thicker channel layer show greater ΔV_{th} due to an increase in the volume in which photoexcitations can occur [269].

3.4.4.4 Control of instability mechanisms

There are several routes through which these instability mechanisms can be reduced owing to the dependence on the defect sites discussed.

The reduction of defects in the dielectric and dielectric/a-IGZO interface is a clear route to reducing instability effects, since fewer defects means fewer charge trap sites and therefore less shift in V_{th}. For the dielectric layer this is achieved by optimising the deposition process. For example, it has been shown that higher temperature (250 °C) ALD deposited dielectric produced more stable devices than identically fabricated devices with lower temperature (200 °C) ALD dielectric [270]. For the interface it has been found that instability is minimised by diffusion of some material at the interface which acts to pacify charge traps at the interface [271]. This interdiffusion can be achieved through post deposition thermal annealing, and significantly reduces device instability.

In addition to reducing charge traps at the interface, which directly affect V_{th}, the other key defects that create the deep-subgap states from which electrons are excited to the conduction band, leaving a hole to be trapped and contributing to the increase in I_{off}, occur at the semiconductor to dielectric interface. As with routes to reducing V_O and metal-metal bonds, the most effective method for reducing these states is post-deposition thermal annealing [272]. This has been shown by many groups to reduce device instability, particularly NBIS [27, 126, 232, 269]. It should be noted that most demonstrations of thermal annealing lead to improved device stability involve

temperatures at the top of, or above, those compatible with polymer substrates (see "Defining "low" temperatures" below).

3.5 Metal oxides of TFTs in a flexible form-factor

Truly flexible electronics has captured the imagination of the public for at least 60 years, with ideas of rollable, foldable displays and technology permeating science fiction and popular culture throughout the second half of the 20th century, back to *The Mechanical Monarch* by E.C. Tubb, published in 1958 [273]:

> *"Against one wall a wide sheet of clear material suddenly flared with light and swirling colour. It steadied and a woman stared from the screen."*

This was followed by other similar ideas, such as electronic newspapers and smart contact lenses, appearing over the following 40 years [274–277], becoming the absolute expectation in science fiction of the 21st century. Academia and industry have been trying to realise this vision for many years, first by thinning down crystalline silicon (c-Si) chips and reducing their size so they appear flexible (although the silicon itself remains rigid), followed by the introduction of truly flexible silicon in its amorphous (a-Si) [23, 278] and low-temperature polycrystalline (LTPS) forms [279, 280], followed by the revolution in organic electronics [281–283]. While excellent electrical performance can be maintained with c-Si, real flexibility is not possible. Conversely, good flexibility is possible with both a-Si and organics, but the electronic functional performance is greatly reduced in comparison to c-Si (mobilities of <1 $cm^{-2}V^{-1}s^{-1}$ and <10 $cm^{-2}V^{-1}s^{-1}$ are reported for a-Si and organics respectively [25]). LTPS does offer good performance in a flexible form, but the manufacturing costs and high processing temperatures make it an unattractive option for most flexible applications.
Metal oxides have provided a route through which truly flexible, high performance, and low cost displays and wider electronic technologies are possible.

3.5.1 Advantages of electronics on flexible substrates

While the appeal of flexible displays for the general public is largely tied to the novelty of such technology, there are many practical advantages to migrating display,

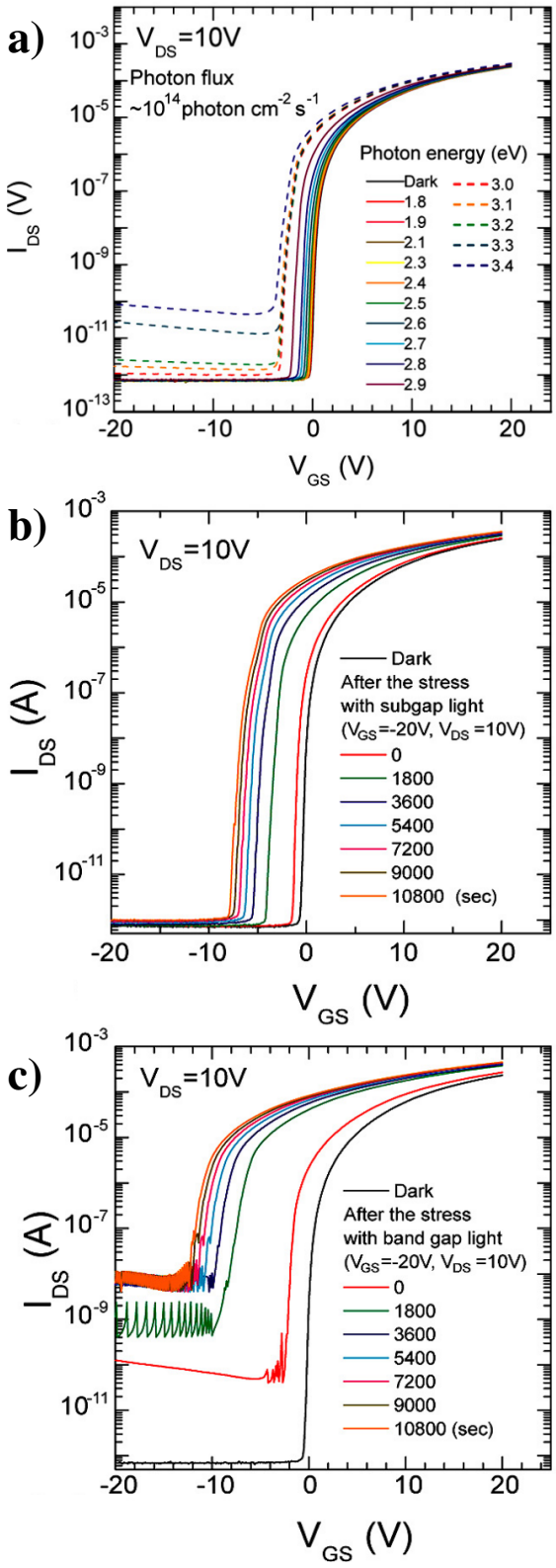


Figure 3.9: **a)** I-V transfer curves for wet-annealed TFT in dark conditions and under monochromated light illumination with various photon energies from 1.8 to 3.4 eV (λ = 700–365 nm). **b)** Variation of transfer curves with subgap photon (E = 2.7 eV) illumination. **c)** Variation of transfer curves with band-gap photon (E = 3.4 eV) illumination. Reproduced from Nomura et al. [216].

communication, and sensing technologies to flexible substrates.

The use of most flexible substrates greatly reduces the weight of devices, particularly displays which have traditionally been based around heavy, rigid glass and silicon, and for which there is a continuing drive for higher resolution, larger screens. This weight reduction, in turn, reduces handling and shipping, as well as production, costs and enables integration in a wider variety of products.

Flexibility can also bring advantages in terms of product robustness. This stems from the ability of the circuits to flex under impact, meaning device interconnects are not broken by small shear forces, such as vibrations.

Flexible, particularly polymeric, substrates do however present difficulties in forming robust interconnects between discrete components in the first place, particularly as the normal methods of wire bonding are not possible due to the elevated temperatures required. Instead there is a great deal of work looking at the use of anisotropic conductive adhesives to make robust interconnects, and this topic is covered in detail by Kim et al. [284] for rigid-to-flexible bonding, although no review yet exists covering flex-to-flex bonding.

A further advantage of flexible circuits is the possibility to integrate functionality into new form factors that are not accessible with traditional, rigid circuits. These can include medical implants [285–288], intelligent packaging [289], wearable devices [290], and artificial skin [285, 291], as well as the aforementioned flexible displays which can be rolled up into a very small size [292–298].

3.5.2 Materials for flexible substrates

There is a wide range of materials on which metal oxide TFTs can be fabricated, in principle the only limitation is the need for a relatively smooth (roughness $<$100 nm at least), continuous area on which the devices can be fabricated. In practice, however, the vast majority of flexible substrates used are polymers, either free standing or laminated onto a glass carrier for ease of processing.

The most commonly used polymers found in literature are polyimide (PI), polyethylene terephthalate (PET), and polyethylene naphthalate (PEN), although many others have also been used. PET and PEN are attractive due to their very low cost, while having good

chemical resistance, reasonable thermal stability below their glass transition temperature (T_g), and good transparency (both have cut-off wavelengths, λ_c in the ultraviolet). Alternatively PI offers similar advantages in terms of chemical resistance and thermal stability (PI is in fact one of the most thermally stable polymers available), while having a significantly higher glass transition temperature, T_g (PI has a T_g of 300 °C compared to 120 °C for PEN and 80 °C for PET). In PI this does, however, come at the expense of transparency as standard PI has λ_c=500 nm, although recent work has lead to the development of colourless PI (CPI) [299, 300].

There have also been reports of TFTs fabricated on paper [301–303], thin metal foils [304–306], and ultra-thin flexible glass [307–309]. While paper and metal foils are clearly not transparent, they do have benefits of low cost and high temperature processing capabilities respectively [310]. Ultra-thin glass, on the other hand, offers both transparency and high processing temperature, along with increased mechanical protection for devices, but at a significantly higher cost and reduced flexibility (the maximum bending radius is $>$1 mm)

3.5.2.1 Defining “low” temperatures

The choice of substrate has a profound impact on the work of this thesis, which here is aimed at improving flexible devices, meaning a flexible substrate is needed. As is discussed above, the most commonly used substrates for flexible devices, and the ones most compatible with the requirements of low cost and high performance, are polymers. This, therefore, puts a fundamental limit on processing temperatures at around 300-350 °C, the maximum processing temperature for high-temperature polymers such as PI. This needs to be considered in the context of the temperatures commonly used in processing of metal oxides to optimise performance, often between 300 °C and 550 °C.

As such, throughout this work, reference to “low” temperatures means those compatible with polymer substrates (i.e. below 300 °C) and “high” temperatures are those above this ($>$300 °C).

3.5.3 Further considerations for circuits on flexible substrates

While there are clearly great advantages to flexible electronics, they bring additional challenges to device manufacturing. There are several additional considerations for fabricating devices on flexible substrates. The most obvious being the flexibility of the substrate itself.

If the substrate is flexible it may be prone to movement during production processes, such as layer deposition. This greatly reduces the accuracy of lithography, meaning design tolerances must be greater, increasing device footprint (and therefore increased defect counts), parasitic capacitance, and overall circuit size. To reduce movement of the substrate it can be held under tension during lithography, but this introduces residual stress in the deposited films which can lead to delamination or cracking in some layers. Alternatively, the substrate can be laminated onto a rigid carrier for fabrication, although this can lead to problems with releasing the substrate afterwards.

Another issue with flexible substrates, particularly polymers, is differential thermal expansion experienced with the different added materials. As noted above, PI is one of the most thermally stable polymers, with a coefficient of thermal expansion similar to that of the materials used to make up the TFTs, making it a good choice to limit this effect.

Another significant effect of introducing flexibility is the effect on performance of devices with bending. This is reviewed by Heremans et al. [311] who show that, for many candidate materials (particularly LTPS and organic semiconductors), bending has a significant impact on carrier mobility. However, a-IGZO shows strikingly little variation with stress [312, 313]. Indeed figure 3.10 shows the variation in threshold voltage, subthreshold swing, on current, and mobility with bending to a radius of 2 mm, where it can be seen that all parameters remain almost constant. This remarkable insensitivity to bending is attributed to the same mechanism that gives IGZO such good characteristics even in the amorphous form - namely the spherically symmetric S orbitals of the cations, as discussed in further detail in chapter 2. This makes a-IGZO an excellent choice for flexible electronics, particularly where they are expected to perform in a flexed state such as in packaging and curved displays.

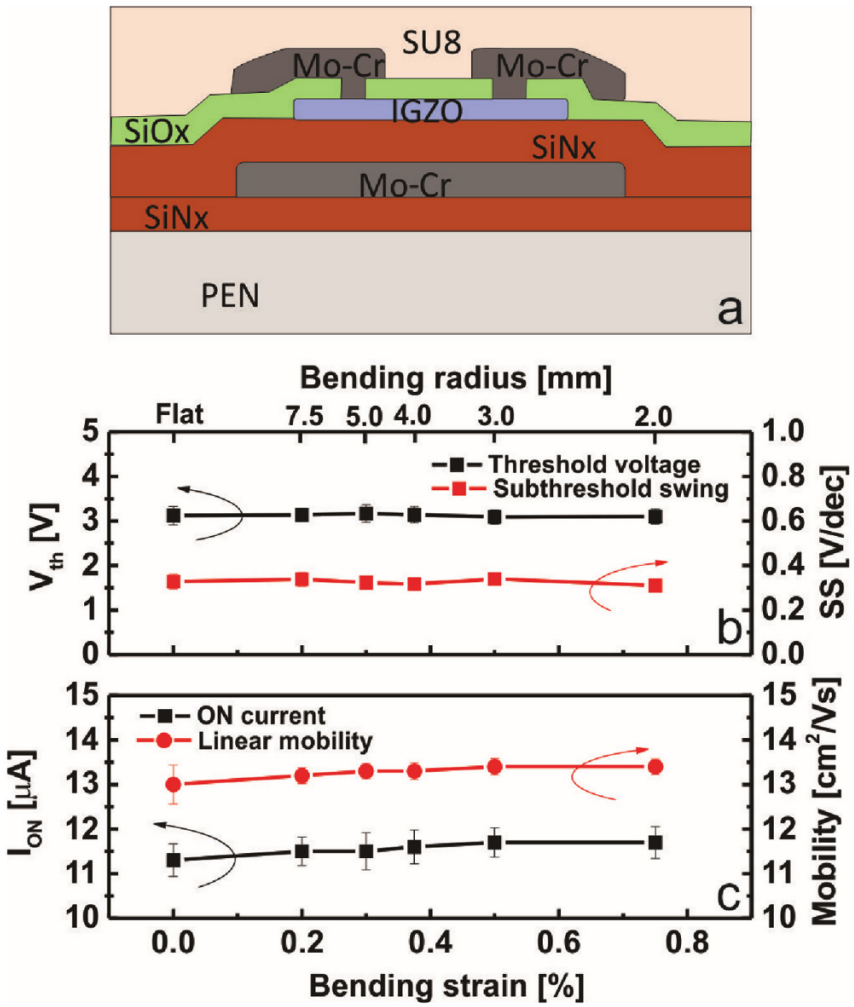


Figure 3.10: Bending properties of a-IGZO thin-film transistors on 25 μm poly(ethylene naphthalate) (PEN): a) device structure and materials used (MoCr for the electrodes; silicon oxide (SiO_x), silicon nitride (SiN_x), and an epoxy photoresist (SU8) are used as dielectrics). b) Threshold voltage and subthreshold swing; c) ON current and mobility as a function of bending strain and corresponding bending radius. Channel length and width of the TFT are 20 μm and 60 μm respectively. Linear transfer curves were characterized at a drain–source voltage V DS = 1 V and gate–source voltage V GS = 10 V. Reproduced from Heremans et al. [311] .

3.6 Applications of a-IGZO and other metal oxide TFTs

The remaining sections of this review consider common applications of a-IGZO and other metal oxide TFTs. Current - and likely future - applications of such materials can be broadly split into two categories - display applications and low cost flexible circuits, with predictions of market values of around $49B and $7B respectively by 2020 [4]. Both applications are covered here, though the discussion of use within display technologies is somewhat truncated, as it is not the focus of this thesis and several comprehensive reviews already exist [314–318].

3.6.1 Display Technology

Display applications have been the driving force in metal oxide, and particularly a-IGZO, TFT development [25]. Indeed, it took just one year from Nomura's demonstration of a-IGZO TFTs in 2004 for the first demonstration of a display backplane (for black and white e-paper) based on a-IGZO TFTs by Toppan Printing Co. Ltd [149], which was shortly followed by an active matrix OLED (AM-OLED) display demonstrated a year later by LG Electronics Inc. [319, 320]. Many other companies then turned to a-IGZO, including Samsung [155, 247], Hitachi [321], and AU Optronics Corp. [322], demonstrating progressively larger displays, as well as LCD back panels. Finally, commercial production of a-IGZO based displays, by Sharp in 2012 [3], started just 8 years after Nomura's initial work.

As discussed above, part of the appeal of a-IGZO for displays comes from the advantages afforded by flexible displays - light weight substrates, increased durability, and the popular appeal of a bendable display, and from the very first demonstrations flexible displays were being considered [149]. However, a-IGZO also has advantages over rival flexible materials (a-Si, LTPS, and organics) beyond just being flexible.

One particular area where a-IGZO outperforms all rivals is transparency. As discussed previously, when deposited on suitable substrates a-IGZO, along with other metal oxide semiconductors, can be used to form fully transparent circuits. If combined with suitable OLED display technology this gives the possibility of displays that are completely transparent in the off state, but when turned on become full displays, see figure 3.11.

The likelihood of this has also recently taken a step forward with a slew of patents to Samsung, which include both transparent and bendable mobile phones [323, 324].

As depicted in figure 3.11**a)**, a-IGZO also outperforms both a-Si and organic transistors in terms of mobility and nearly matches that achieved with LTPS [325]. This relatively high mobility, the origin of which is discussed in chapter 2, allows devices with high operating frequency capable of driving high frame rate displays.

While LTPS matches or beats a-IGZO in mobility and operating frequency, this comes at the expense of a higher processing temperature (>350 °C) and significantly reduced uniformity, making it an unsuitable choice for ever larger display screens. Organics, too, suffer from a lack of areal uniformity due to the solution based processing used to deposit them over large areas. Uniformity is particularly important in display applications because the output of a given OLED pixel is highly dependent on the driving TFT's characteristics - it has been reported that a variation in threshold voltage of just 0.1 V can lead to up to a 20% variation in that OLED pixel's luminosity [250, 326].

3.6.2 Logic, sensing and communication applications

Alongside the development of a-IGZO for display applications, work has been ongoing looking at a-IGZO and other metal oxides for applications such as logic circuits, sensing, power transmission, and wireless communication [25]. The advantages of metal oxides in these areas are similar to those for display applications but for somewhat different reasons. For example, large area uniformity now enables large volume of consistent device production rather than large area displays; transparency facilitates creation of non-visible circuitry for, for example, security applications; flexibility allows integration of devices into previously inaccessible form factors while increasing the mechanical durability of circuits; and the low cost of production allows access to markets for which silicon-based devices are too expensive (such as fast moving consumer goods (FMCGs)).

3.6.3 Logic circuits

The development of metal oxide circuitry started a few years after the rapid growth in metal oxide research, in the years around 2000, with Presley et al. demonstrating the first

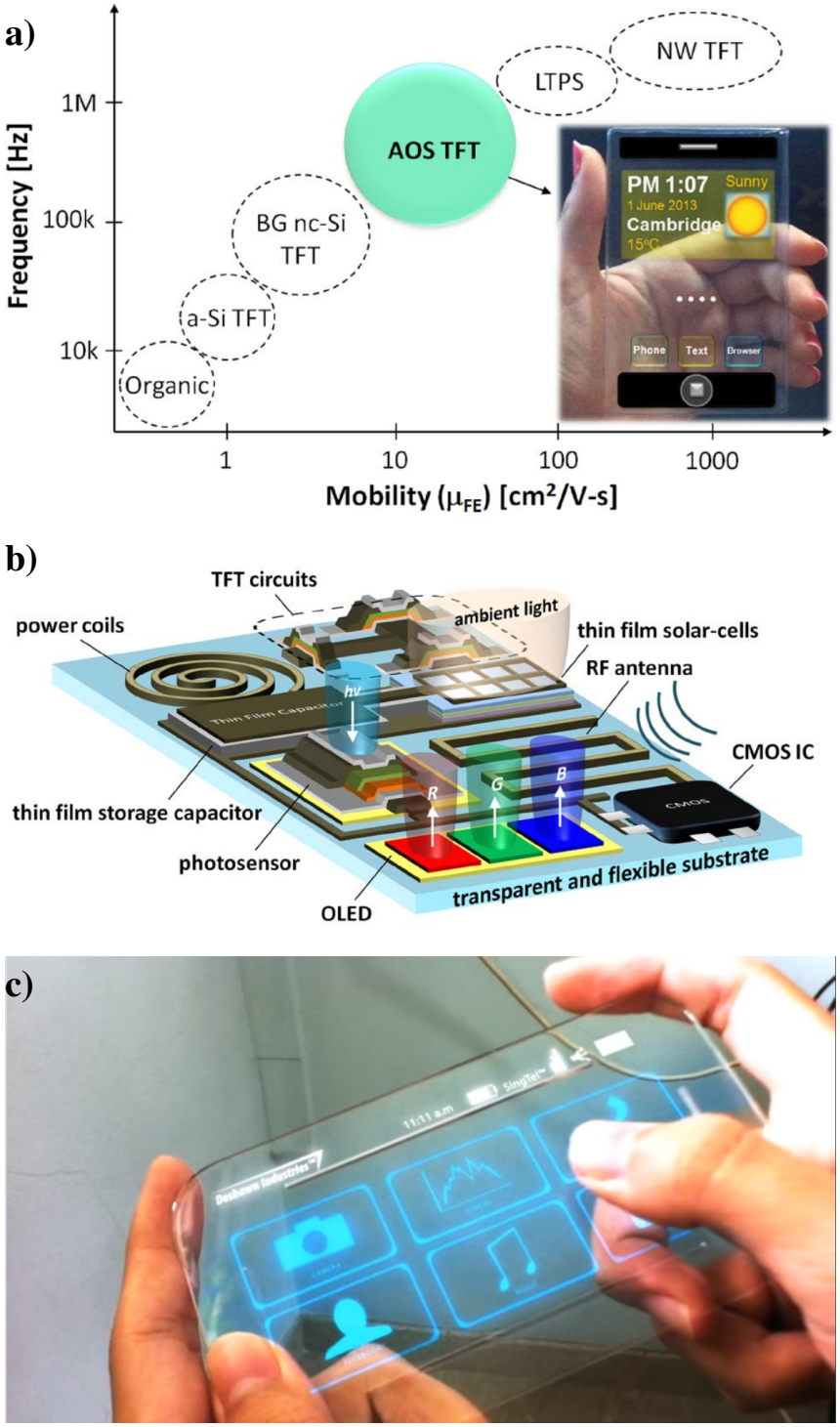


Figure 3.11: **a)** Materials for TFTs showing a mapping between mobility and frequency capability. Inset: conceptual image of a transparent smart phone. **b)** Conceptual illustration of future transparent and flexible systems where display elements, sensors, circuits, RF functionality, and energy devices are heterogeneously integrated using oxides and other thin film technologies, including silicon CMOS. Here, for better illustrative purposes, transparency is disregarded. **a)** and **b)** Reproduced from Lee et al. [317] with data compiled from [2, 26, 107, 318, 327–333]. **c)** Still of a transparent PDA device featured in the film Iron Man 2 [334].

fully transparent circuits based on IGO in 2006 [335]. This circuit, similar to most early circuitry, comprised a ring oscillator made of an odd number of inverters (in this case 5), connected in series as in figure 3.12**b)**. Each inverter, in turn, comprises a control TFT and a load (either a second TFT or a resistor), figure 3.12**a)**. The use of ring oscillators allows measurement of propagation delay, which is widely used as a benchmark for the maximum operating speed of a TFT [336]. The initial work by Presley produced relatively poor results, with the 5 stage oscillator operating at 9.5 kHz, corresponding to a stage delay of 11 μs/stage, largely due to significant parasitic capacitance arising from the large source/drain to gate overlaps.

Shortly after the demonstration from Presley, Ofuji et al. demonstrated a similar system, this time using IGZO TFTs and significantly smaller overlaps, achieved 410 kHz, equating to a propagation delay of 0.24 μs/stage - half that reported for a-Si:H [337] and one third for organic TFTs [338].

Since this early work, further improvements in speed have been seen, as well as increased complexity (for example shift registers [339] and scan drivers [340]) and implementation of devices on flexible substrates still able to yield good performance. See for example the demonstration from Mativenga et al. of an 11 stage ring oscillator made of a-IGZO TFTs on PI/PET substrates, with a propagation delay of just 0.48 μs/stage [341] in figure 3.13, and their later demonstration of high performance shift registers on PI which are still operational while rolled to a radius of just 4 mm, figure 3.14. Indeed, these improvements have lead to demonstrations of full microprocessors, initially using crystalline IGZO [342–344], and recently with an amorphous metal oxide on flexible substrates reported by PragmatIC and ARM Holdings [5, 345].

3.6.4 Sensing

Alongside the development of logic elements, many groups have looked at the application of metal oxide to sensing [25]. Sensing capabilities are attractive as they open up possibilities within many more areas, including smart implants [347], artificial electronic skin [348], food safety [349], and temperature monitoring [350–352]. These sensors are in the early stages of development, but show great promise in a research setting and are now being integrated into industrial production.

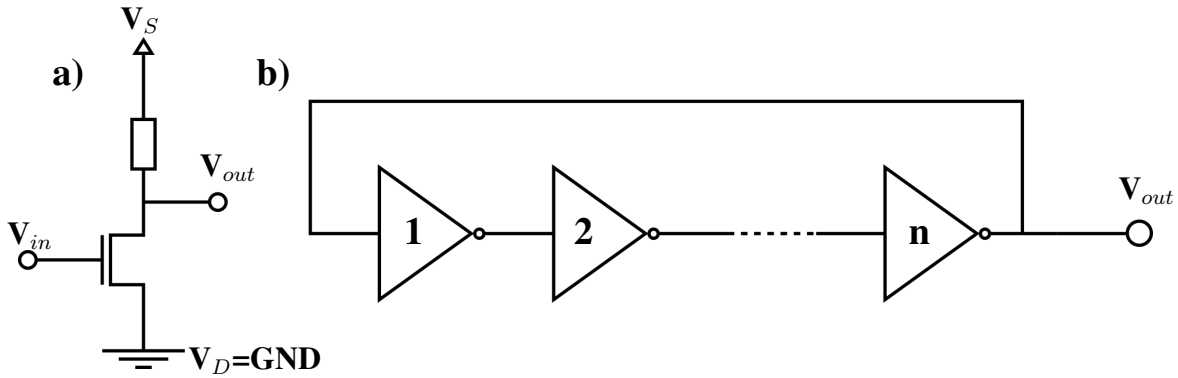


Figure 3.12: **a)** Simple NMOS inverter with a resistive load, the resistor can be replaced by a second TFT wired as a diode (gate and drain shorted together). **b)** Ring oscillator using n inverter stages where n is always odd.

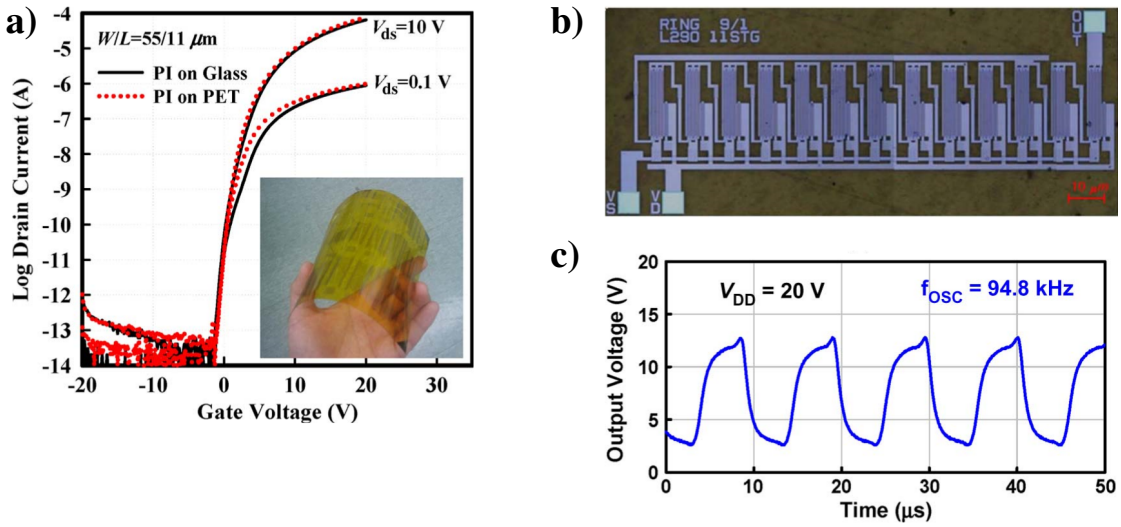


Figure 3.13: **a)** (Insert) Optical image of a fabricated flexible sample and the transfer characteristics of an a-IGZO TFT before and after detachment from glass to PET followed by annealing for 2 h in vacuum at 150 °C. **b)** Optical image, and **c)** output characteristics of the fabricated ring oscillator. Reproduced from Mativenga et al. [341]

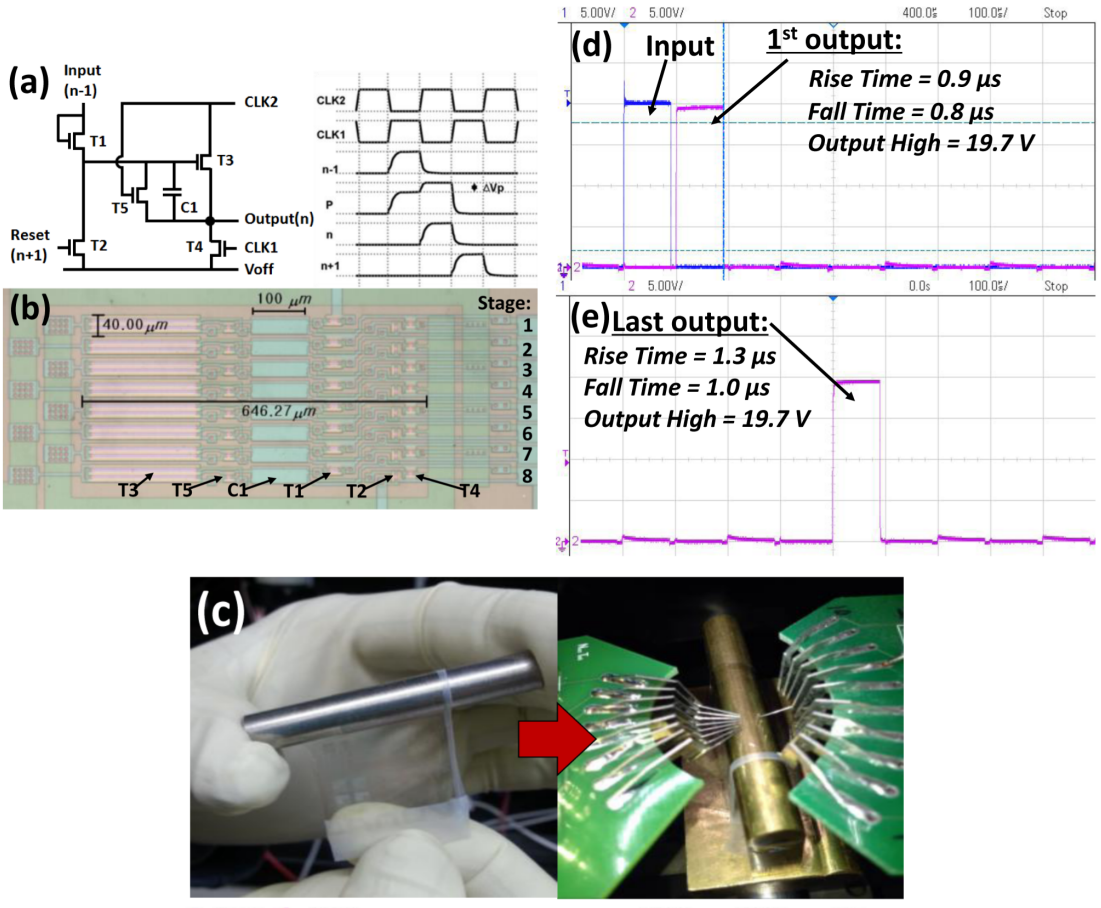


Figure 3.14: Operation of a fully transparent and rollable a-IGZO TFT shift register (SR): **(a)** One stage circuit schematic and timing diagram of the two-clock, five transistor (5T), and one capacitor (1C) SR; **(b)** optical micrograph of a measured eight-states SR; **(c)** image of the sample containing the SR as it being rolled to a cylinder and the measurement set-up for the SR, while under bending stress. **(d)** and **(e)** First output and last output of the eight-stage SR under bending radius of 2 mm for input voltage VDD = 20 V. All rV$_{th}$eproduced from [346]

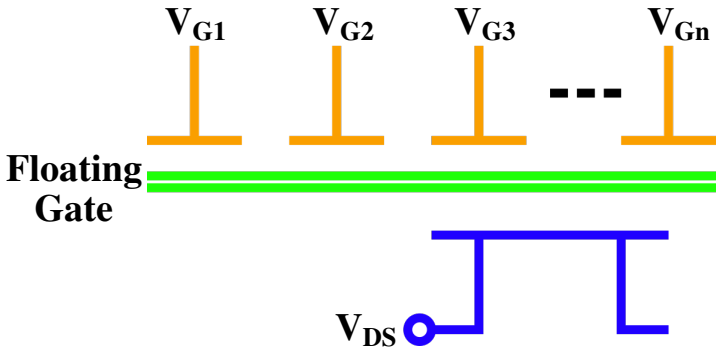


Figure 3.15: Schematic image of the capacitive network of a flexible neuromorphic transistor. The carrier density of the channel is modulated by the weighted sum of all inputs of sensing gate and control gates. Adapted from Liu et al. [353]

Metal oxide sensors broadly operate along one of two lines: either multiple sensing and control gates are inductively coupled to the TFT gate, as in the work from Liu et al. [353], see figure 3.15, or a sensing surface (an externally coupled membrane [354], the TFT gate [352, 355], or even the channel layer [356–358]) interacts with the local environment, ad/absorbing gas or liquid molecules, creating a shift in potential or electrical characteristics of TFT.

An alternative route to sensing applications takes the form of integrating metal oxide circuitry with existing analogue sensors. For this metal oxide based analogue to digital converts (ADCs), comprising comparators and surrounding logic, need to be integrated with existing bio-sensors. Practical demonstrations of this have recently been shown [359, 360], however widespread implementation is limited by device variability, both between devices and as device performance changes due to stability issues. Such systems are particularly sensitive to variability as the comparators here compare an input signal to a reference voltage, and so any variation in threshold characteristics directly translates into a variable output of devices. These applications highlight the need for truly stable and uniform devices.

3.6.5 Energy Harvesting

In order to leverage the low cost functionality made possible with a-IGZO technology, a power source is needed. In high value applications typically suited to silicon technology, this can be supplied by either a fixed supply or an integrated battery. This is, however,

associated with high cost (both traditional coin cell batteries and next generation printed carbon batteries have a price floor one or two orders of magnitude greater than the cost per circuit for a-IGZO systems) and reduced flexibility (traditional batteries are rigid, while new printed batteries are much greater in size than the circuits being produced). This leaves only the option of supplying the power externally with contactless transmission.

Contactless power transmission can be realised using two inductively coupled coils (source and receiver) and a rectifying circuit to convert the AC input to a usable DC power supply. The receiving coil can be either a traditional metal coil, commonly used in current RFID tags, or if transparency is desired can be a TCO (typically ITO) although this comes at an efficiency cost. The rectifying circuit may be a diode or simply a TFT in diode load configuration (where the gate and drain are shorted together) [361].

If a diode is used it may be one of several different forms. Most reminiscent of traditional silicon diodes is the p-n junction diode, in which a p- and an n-type semiconductor are in contact forming a p-n junction, for example NiO and IGZO as the p- and n-type materials respectively demonstrated by Münzenrieder et al. [362], as well as many other combinations [181, 363, 364]. Alternatively, Schottky diodes with a metal-semiconductor junction are possible. However, due to the large electron affinity of most metal oxide semiconductors only a small Schottky barrier is possible [310]. Still, Chasin et al. successfully demonstrated Schottky diodes using a-IGZO with a Pd contact [365], as did Zhang et al. using an Al contact [366]. Additionally, metal-insulator-semiconductor (MIS) [367], Metal-insulator-metal (MIM) [368], and self-switching diodes (SSD) [369–371] have all been demonstrated, although each has limitations that currently restrict them to academic interest, rather than practical application.

The most efficient and most common arrangement for this rectifying circuitry is the bridge rectifier shown in figure 3.16. This uses 4 diodes (or diode load configuration TFTs) to harness both the positive and negative part of the AC waveform. Using this configuration with p-n diodes, Münzenrieder et al. achieved a DC voltage of 2.1 V at an input frequency of 125 kHz and peak-to-peak voltage (V_{PP}) of 12 V [362], while Chen et al. increased this to around 2.5 V up to 27 MHz with a V_{PP}=8 V using Cu_2O instead

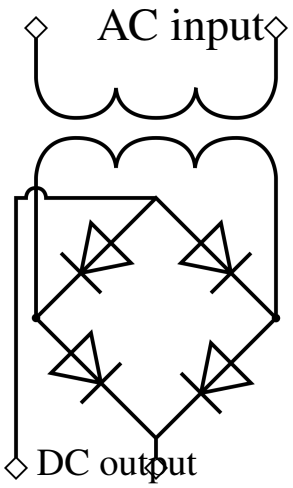


Figure 3.16: Circuit schematic of a bridge rectifier using 4 diodes or diode load TFTs.

of NiO [372].

Using Schottky type diodes in this same configuration, Chasin et al. demonstrated the significant speed advantage inherent in Schottky devices, showing a DC voltage of 1.7 V for an input V_{PP} of just 3 V up to a remarkable 1.1 GHz [373].

Using diode loaded a-IGZO TFTs Kawamure et al. showed a DC voltage around 5 V for an input V_{PP} of 20 V up to at least 25 MHz, showing even diode loaded a-IGZO TFTs are capable of rectifying well above the threshold of 13.56 MHz required for RFID purposes, while being able to operate at sufficiently high voltage to power a display [374].

3.6.6 Data Storage

Data storage is one of the last remaining areas needed to create fully integrated wholly a-IGZO based systems. As such, much recent work has focused on non-volatile a-IGZO memory.

Suresh et al. and Zhang et al. both used charge storage in the dielectric to create multilevel memory storage. Suresh achieved this by doping the AlO_x date dielectric with Pt nano-particles, showing charge retention on the order of a few hours [375], while Zhang achieved this by creating a double layer of IGZO separated by a thin Al_2O_3 charge tunnelling layer, with charge retention of around 1 day [376]. Both of these systems essentially leverage the creation of charge trapping defects, discussed above, to create hysteresis in the a-IGZO TFT behaviour, which is then used as a way of storing

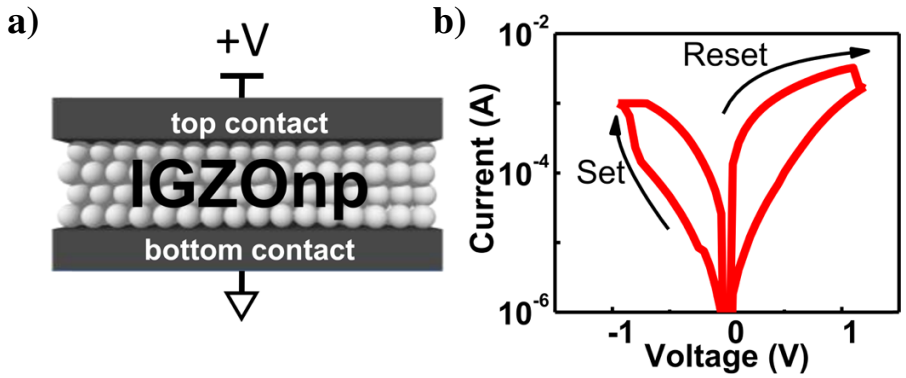


Figure 3.17: **a)** schematic of the memristor device and **b)** representative IV characteristics of the set and reset process. Reproduced from Rosa et al. [378]

information.

Van Breemen et al. utilised ferroelectric dielectric behaviour (see sections II and III of the review from Petti et al. for discussion of ferroelectric behaviours [25]) showing a 16 $\times$ 16 IGZO TFT array using ferroelectric P(VDF-TrFE) gate dielectric, with retention times up to 12 days [377].

Memristors have also been considered as a route to achieve stable data storage, as demonstrated by Rosa et al. [378] with solution processed a-IGZO, figure 3.17. Here conducting filaments are induced in the a-IGZO material during the writing phase, which are then disrupted during the reset phase. This system showed data retention again on the order of a few hours.

In addition to these and other emerging implementations of metal oxide memory, work is ongoing to create hybrid systems combining metal oxides with other existing technologies to meet memory requirements for many different applications. These are not discussed here but are covered well in recent reviews by Wong (looking at Metal-Oxide resistive switching RAM (RRAM)) [379], Zhao (looking at high-k dielectric non-volatile memory) [380], Meena (looking at the general field of new non-volatile memory technologies) [381], and Sacchetto [382] and Mladenov [383] (looking at memristor technology).

3.6.7 RFID/NFC Communication

One of the most promising applications of a-IGZO outside of display technology is high volume, lost cost, and disposable wireless communications systems such as RFID/NFC

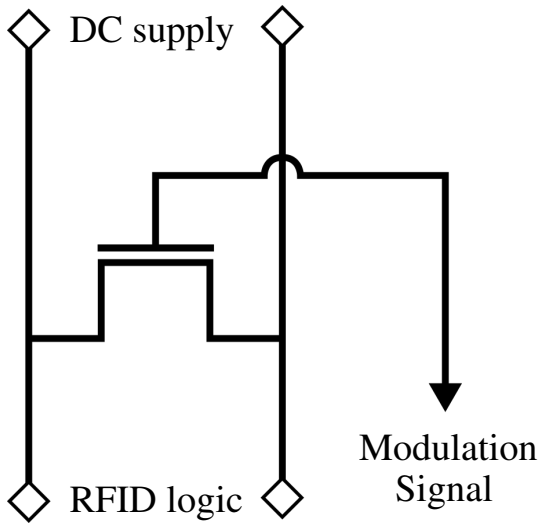


Figure 3.18: Schematic of the load modulator used to encode signal in RFID tags.

tags [384]. As well as the low cost, tags based on a-IGZO benefit from their flexibility, allowing integration in packaging, clothing, and in multiple different form factors, as well as the potential for being non-visible, allowing integration into windows, mirrors, and food packaging [25]. Building on earlier designs for organic RFID tags [385–387], Ozaki et al. first demonstrated a fully a-IGZO based RFID tag working at 13.56 MHz in 2011 [384, 388], which has now been replicated by many other research groups on both rigid and flexible substrates, including fully transparent versions [191, 389, 390].

One remaining component of the RFID tag, not discussed above, is the load modulator. This is simply an additional TFT placed directly in the DC power supply line, with the RFID code encoded to the gate voltage see figure 3.18. By modulating the gate of this TFT with the code, the DC supply is turned on and off, altering the power consumption of the tag and therefore the power harnessed by the tag's receiver coil. This modulation in power consumption in turn creates fluctuations in the electromagnetic field which can be read by the RFID reader and decoded into the data to be transferred.

3.7 Conclusion

The aim of this chapter has been to familiarise the reader with both the development of metal oxide electronics, in particular a-IGZO devices, and the variety of applications to which a-IGZO is now being applied. It is clear that a great deal of work has gone

into the development of these systems, particularly over the last 15 years, with great strides being made in understanding of the fundamental physics of metal oxides, potential applications in a wide variety of sectors, and importantly understanding of the current limitations particularly due to native and induced defects.

The motivation for the remainder of this work draws primarily from this discussion of defects, in section 3.4, with the aim of improving device performance through reduction in defects, and a specific focus on applications in flexible circuitry such as RFID tags.

Chapter 4

Sample and Device Fabrication

Throughout this work, several different processes and techniques were used for sample fabrication. The details of these processes are set out in this chapter, covering first the thin-film deposition techniques, followed by the steps used to define device structures. Included in this chapter are details of the techniques, discussion of the parameters used throughout this work, and consideration of the particular constraints dictated by the involvement of the industrial project partner.

In this work both full transistor devices and unpatterned stacks of materials have been studied to provide insight into the connection between material structure and the electronic properties of devices. As such, some of the samples studied did not receive all of the following preparations; this is made clear during discussion of such work.

4.1 Thin-Film deposition methods

4.1.1 Sputtering

Most of the thin-film materials here were deposited by sputtering. The basis of sputtering is the bombardment of a target of the desired material with charged ions, creating a vapour of the target material which is then deposited as a film on a substrate, figure 4.1. Many different materials can be sputtered, including metals, metallic compounds, and metal oxides. In this work all device layers, other than the gate oxide, were deposited via sputtering, with sputtering parameters discussed where appropriate.

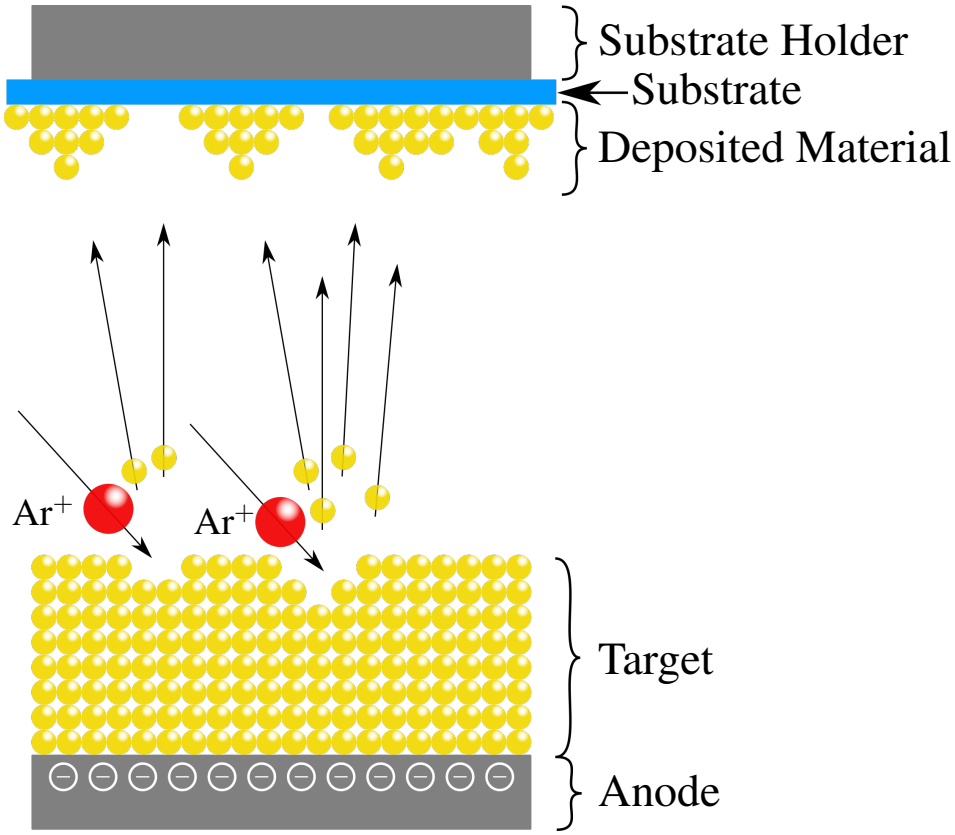


Figure 4.1: Schematic illustration the sputtering process. Large argon ions accelerate towards the negative anode and impact the target, ejecting target atoms which travel through the sputtering chamber, getting deposited on the substrate.

The properties of the deposited film can be tailored through variation of several variables that determine the sputtering process. These include substrate temperature, chamber base- and working-pressure, sputtering power, distance between the target and sample, target composition, the power applied, and substrate bias. The following sections describe the effect of these variables and the conditions used in this work.

4.1.1.1 Effect of Substrate Temperature during Sputter Deposition

Substrate temperature affects the effective rate of deposition, the film growth mechanisms and hence the structure of the final films. When sputtered species hits the substrate they are adsorbed onto the surface with some sticking probability. This depends on the temperature of the substrate as well as the energetics of the adsorbed atom and the amount of the material already present [391,392]. If the atom is adsorbed directly onto an aggregate of other deposited atoms, it will remain there as long as the aggregate remains

stable. If adsorbed onto the substrate surface it may diffuse across the surface until it reaches an aggregate or is desorbed, or it may stick to the substrate creating a new nucleation site. Where enough atoms aggregate a critical nucleus size can be reached at which point the aggregate becomes stable (i.e. the Gibbs free energy is stable with respect to the size of the nuclei, $\partial \Delta G / \partial r = 0$). The radius of such an aggregate, r^*, is given as [391]

$$r^* = \frac{-2(a_1\sigma_{v-c} + a_2\sigma_{s-c} - a_2\sigma_{s-v})}{3a_3\Delta G_v} \tag{4.1.1}$$

where $a_{1,2,3}$ are constants describing the area of the aggregate exposed to the atmosphere, in contact with the substrate, and its volume respectively, $\sigma_{v-c,s-c,s-v}$ are the condensate-vapour surface, substrate-condensate interface, and substrate-vapour surface free energies respectively, and ΔG_v is the Gibbs free energy of condensation of the material. The role of substrate temperature in nucleus formation can be seen by taking the derivative of equation 4.1.1 with respect to temperature, and using the assumptions set out by Neugebauer in [393], to show that

$$\left(\frac{\partial r^*}{\partial T}\right) > 0 \tag{4.1.2}$$

as long as $|\Delta G_v| < 1.64 \times 10^{10}$J m^{-3}, which is the case where a nucleation barrier exists. Equation 4.1.2 indicates that increasing the substrate temperature increases the critical nucleus size. In turn, the size of this critical nucleus significantly affects the nature of the film growth. When critical nucleation occurs, and the nucleus grows beyond this size, and islands are formed that grow as more atoms are deposited. If r^* is large the size of the islands, both in-plane and out-of-plane, and the separation between islands is large, so more material must be deposited before a continuous film is achieved. As these islands grow, they impinge on one another, either joining to become a single homogeneous island, or creating a grain boundary. As further material is deposited these islands grow until a continuous film is formed and further material is deposited at a consistent rate across the substrate. The structure of these large islands may remain evident in the topography of the film surface, up to thick films of a few micrometers, see figure 4.2. This is known as island, or Volmer-Weber, growth [394]. When r^* is small, in the limiting case where r^* is less than the radius of the deposited atoms, there is an initial large population of critical and supercritical nucleations. Subsequently many small islands are formed, leading to

rapid formation of the continuous film, and layer by layer growth, known as Frank-van de Merwe growth [395–397]. These factors suggest that lower substrate temperatures should be used where smooth, homogeneous films are desirable, particularly when the films are also very thin, on the order of tens of nanometers.

In this work both the quality and structural uniformity of the sputtered films is important, and so substrates were held at room temperature throughout sputter deposition.

A final consideration, with regard to temperature in sputtering, is local heating of the substrate during deposition caused by the transfer of kinetic energy from the deposited atoms. To mitigate this, the sputtering power and kinetic energy of the deposited material, section 4.1.1.8, must be controlled. In addition, there may be some further heating through the impact of secondary electrons generated at the target, and high energy primary electrons from the cathode escaping from the plasma region, which can account for up to 50% of substrate heating during sputter deposition [398, 399]. To reduce the effect of this the substrate may be negatively biased to repel the electrons, see section 4.1.1.9.

In this work, the samples were attached to a large metal carrier which acts to quench any local heating effects and a negative bias applied.

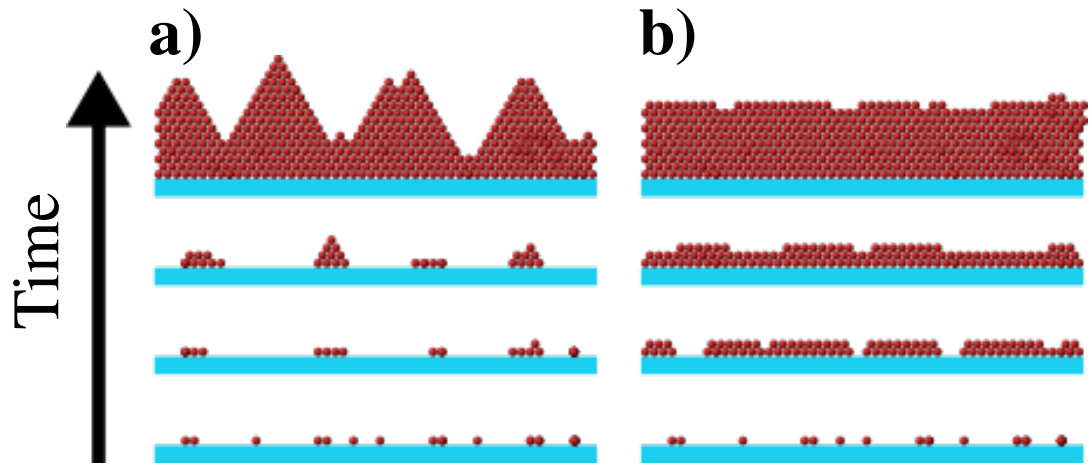


Figure 4.2: Schematic illustration of the growth of a film through sputtering. a) demonstrates island type, or Volmer-Weber growth [394]. b) demonstrates layer-by-layer, or Frank-van der Merwe [395–397] growth. The presence of the island structure persists even up to relatively thick layers of a few micrometers.

4.1.1.2 Effect of Sputter Chamber Base-Pressure

The base pressure of the sputtering chamber is the pressure of the chamber before the introduction of sputtering gases. The lower the base pressure, the lower the presence of contaminants in the chamber which could be incorporated into the deposited material and potentially degrade the physical and electrical properties. However, this desire for a low base pressure must be balanced against the constraints of vacuum technology, and the need for a reasonable throughput in a commercial setting. Therefore, an acceptable value for the base pressure must be sought for the equipment being used and the requirements of the process. In this work a maximum base pressure of 1 mPa was used for all depositions unless otherwise stated.

4.1.1.3 Effect of Sputter Chamber Working-Pressure

The working pressure of the system defines the pressure when the sputtering gas has been introduced. The gas is normally either a pure argon gas, or a mixture of argon and some reactive species such as oxygen, nitrogen, or methane. This gas is introduced to the system in a continuous stream, through a variable throttle value, and the system continuously evacuated using a diffusion pump to maintain the desired working pressure. This continuous introduction and removal of the gas is used so that the products of any outgassing from substrate, target, or the chamber itself are removed quickly, and therefore do not act as impurities during deposition [391].

The gas facilitates sputtering but also introduces scattering sites that affect the deposition of the sputtered target atoms. That is, when a species is ejected from the target, it travels in a straight line until it hits a scattering site or the substrate. This means that, when there are no scattering sites, material travels directly from the target to the substrate, arriving at normal incidence (or close too) depending on the gun angle relative the the substrate. This creates a very uniform layer, with low surface roughness (provided the arriving atoms do not desorb or disturb other adatoms, see the discussion of accelerating voltage below). If structures are already present on the substrate, the deposition builds only on the top of the structures. However, in the presence of gas scattering centres the atoms scatter and impinge the substrate at many different angles. Then, where structures are already present,

the film forms both on the top and side walls of such structures, and causes increased roughness. This growth of a film on the side walls can cause dimensional changes, such as channel shortening, which are detrimental to device performance. Therefore, ideally there should be no scattering centres.

However, this is balanced by the need for argon gas as the source of sputtering ions and to maintain a plasma, and in reactive sputtering the need for chemical reactivity. This leads to a balance being found where sufficient gas is present to facilitate sputtering, but the minimum amount is used so as not to introduce excessive scattering centres. This point is generally taken to be a pressure at which the mean free path of the atoms is a tenth, or less, the size of the chamber [391].

In this work a working pressure of 500 mPa was used for all depositions unless otherwise stated. For IGZO deposition in this work a total gas flow rate of 90 sccm was maintained with variable O_2 partial pressures.

4.1.1.4 Reactive Sputtering

Reactive sputtering is the process of depositing a compound material, such as an oxide, carbide, or nitride, by sputtering an unreacted, or partially reacted target in an atmosphere containing a reactant gas, such that the sputtered atoms react with the gas immediately before being deposited on the substrate [400].

In this work aluminium oxide was deposited from an aluminium target in an argon-oxygen atmosphere for reactive sputtering, while IGZO is deposited from an IGZO target in an atmosphere containing a variable oxygen content, that was used to control the total oxygen content of the deposited film.

4.1.1.5 Effect of Gas Partial Pressure during Sputtering

In addition to the working pressure, when reactive sputtering is employed the partial pressure of the reactant gas is a variable. Partial pressure here means the pressure of the reactive gas as a contribution to the total pressure of the system. This is often quoted as the ratio between the argon and the reactive gas, since the total gas flow-rate and working pressure are kept constant.

4.1.1.6 Effect of Target-Sample Distance within the Sputter Chamber

The effect of the target to sample distance is related to the effects seen with chamber working pressure, above. The greater the separation between the target and the sample, the greater the chance of a sputtered species interacting with a scattering centre. Thus larger working distances can be disadvantageous.

The divergence of the sputtered species from the normal also becomes more noticeable as the working distance is increased. This effect can be useful when coating a large area from a small target, as the areal coverage is increased, but this is associated with reduced areal uniformity with the central region getting more material that the fringes. Where the effects of side wall coverage are undesirable, as discussed previously, a large working distance can be advantageous. During the travel from target to substrate, any material travelling off normal from the target will diverge away, leaving only material traveling on the normal to reach the substrate, thereby reducing side wall coverage. This can, however, only be achieved as long as a sufficiently low working pressure can be maintained so that scattering is minimised.

Where scattering cannot be minimised by having a sufficiently low working pressure, a shorter working distance can be used to reduce scattering and so produce more uniform deposition.

4.1.1.7 Effect of Sputter Target Composition

In the case of sputtering single element targets, consideration of the target composition is limited to the manufacturing purity with most targets available in very high purities, around 99.99% or better. However, for sputtering alloys, complex oxides, or other multi-component materials, the composition of the target becomes a parameter that can variably affect the composition of the deposited film. For the deposition of such complex materials, two options exist - either the target can be manufactured to the desired composition for single target sputtering, or multiple single element targets can be included in the system to allow co-sputtering. In either case it should be noted that elements show some variability in sputter rates which must be accounted for when designing the sputtering process. Where individual targets are used to co-sputter a

compound, the size of each target should be chosen to accommodate differences in sputter rates. Whereas it has been shown that for a mixed target, initial sputtering will favour the deposition of the elements with a higher sputter rate, but after some time (commonly referred to as "burn in") a steady state is reached in which the target is sufficiently depleted of the high sputter rate material that the deposited films actually show the same composition as the target within just a few atomic percent [401].
In this work the deposition of aluminium oxide was done from a single element target with 99.99% atomic purity, with the aluminium oxide being formed by reactive sputtering (see section 4.1.1.4), while the IGZO was deposited from a ceramic target with composition ratio of 1:1:1:4 In:Ga:Zn:O. This composition was used as it matches the desired IGZO film composition, although it should be recognised that the sputter rates of indium, gallium, and zinc do differ, leading to some small variation in film compositions during early depositions. Both targets are treated with an initial burn in period upon installation in the machine to remove any environmental contaminants and, in the case of the a-IGZO target, reach the correct deposition rate for all elements of the target. In addition, each target receives a short additional burn in prior to deposition to remove any additional oxide layer or contaminants introduced during sample transfer.

4.1.1.8 Effects of Sputtering voltage and Currents

The accelerating voltage is the voltage bias between the target and earth. This bias creates an electric field, **E**, that accelerates the sputtering ions before they hit the target. The energy of these ions is determined by the size of the electric field, and has several aspects to consider; the ions must have sufficient energy to initially cause sputtering, called the threshold energy, which is the point at which incident ions have sufficient energy to break the bonds holding surface atoms to the target, this is in the region of four times the heat of sublimation for a target, normally around 15-30 eV [402, 403]. There then exists a region, from the threshold energy up to around 100 eV where the sputtering yield, S, (the ratio of the number of atoms sputtered to the number of incident ions) increases as $S \propto E^2$, followed by a region from 100 eV to between 10 and 100 keV, where S goes as $S \propto E$ as the incident ions collide with the surface atoms and the number of atoms sputtered is proportional to the ion energy [398]. Above this, the ions penetrate into the target,

dissipating some of their energy, and thus reducing the sputtering yield [404].

In addition to the consideration of the ion energy with regard to sputtering yield, the ion energy is the governing factor in the energy of the sputtered atoms when they are deposited at the substrate [405], thus the accelerating voltage, via its control of electic field and therefore the ion energy, is an important controlling factor for the energy of sputtered atoms as they are deposited.

In the linear sputtering region discussed above, where S$\propto$E (and therefore S $\propto$ accelerating voltage), the sputter rate increases linearly with bias voltage. The number of ions impacting the target, the current, is a greater determinant of the sputter rate, as shown by Schuetze et al. [406] with their work on tantalum sputtering, see figure 4.3. Therefore, to increase sputter rates, the current should be increased while the voltage is kept in the optimal range [391].

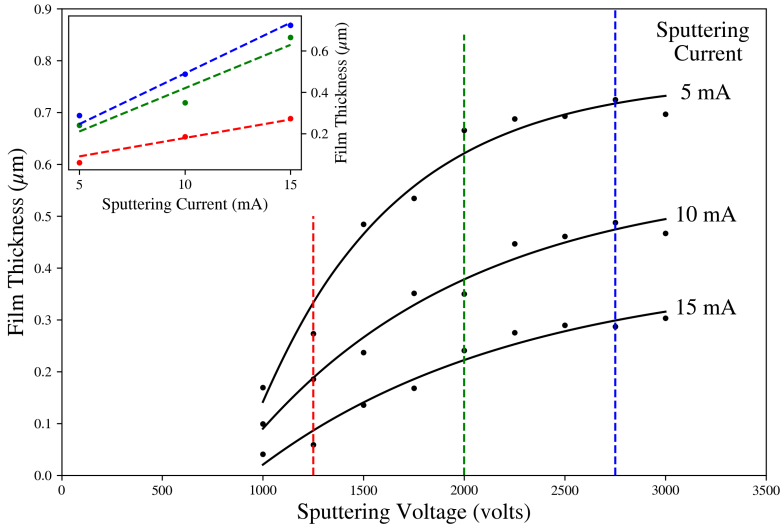


Figure 4.3: Deposition rate of tantalum films vs. voltage at constant current. Reproduced from Schuetze [406]. Inset the deposition rate of tantalum films vs current at constant voltage, extracted from the main plot at the corresponding lines.

4.1.1.9 Effect of Substrate Bias during Sputter Deposition

During deposition the substrate can either be left at a floating potential, reducing the likelihood of resputtering from the sample surface but also potentially leading to charging as the substrate is bombarded with secondary electrons from the target, or can

be deliberately negatively biased. This negative bias has two effects during sputtering; the first effect, briefly mentioned above, is to repel secondary electrons produced at the target which can lead to local heating effects at the surface of the substrate, degrading the deposited material as discussed previously. The second effect is to facilitate resputtering of material from the substrate. That is, the negative bias attracts errant ions, accelerating them towards the sample and displacing material that has been deposited. This resputtering effect can be advantageous in some situations, particularly when high purity single species materials are being deposited, as it can help to remove incorporated contaminants such as carbon or oxygen. However, where multicomponent materials are being deposited, particularly metal oxides, this effect can lead to degradation of the material, particularly its electronic properties. As such, many groups have shown, when depositing metal oxides an optimal value for substrate bias is found by balancing these effects. For a-IGZO this optimal value is between around 90 V and 130 V [407, 408].

4.1.1.10 Experimental detail of Sputter Deposition

For sputter deposition throughout this work, a System Controls Technology horizontal sputter system is used. This is equipped with a 24 slot load lock capable of holding up to 360×465 mm substrates, and has 4 different targets loaded into two connected chambers, see figure 4.4 for a schematic of the system. During deposition, substrates are moved back and forth in front of the target to create uniform films of material, and are held at a constant distance from the sputtering target of approximately 30 mm.

4.1.2 Atomic Layer Deposition

Atomic layer deposition (ALD), is a sequential reactive chemical process, designed to deposit material in a stepwise fashion. Individual precursor chemicals are introduced to a reaction chamber one at a time, as a low density vapour. These chemically interact with the surface of a substrate and, in the ideal case, saturate the available binding sites to cover the surface with single molecular monolayer of precursor. Excess material and chemical remnants are then removed and a second precursor, or reagent, is introduced to react with the initial monolayer, forming a highly conformal monolayer of the desired material, shown schematically in figure 4.5. The prototypical ALD material is aluminium oxide, in

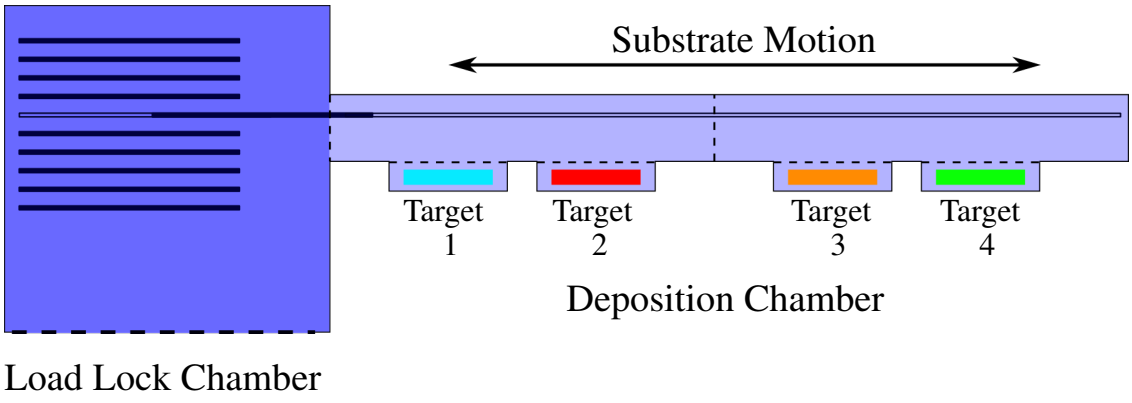


Figure 4.4: Schematic of the sputtering system used throughout this work, viewed from above. Substrates are held on pallets in a load lock chamber and passed into the sputtering chamber one at a time. The dotted lines indicate independently controlled shielding and hatches.

which trimethylaluminum, TMA ($Al_2(CH_3)_2$ - a dimer of two units each consisting of an aluminium atom core with three methyl groups attached) acts as Precursor A and water (H_2O) acts as Precursor B. Both are carried in a continuous stream of nitrogen gas. This type of ALD system was used throughout this work and greater detail can be found in the comprehensive reviews by Puurunen [409] and by George [410]. Within the ALD process there are multiple important variables that determine the deposition process, including temperature, pulse and purge times for the precursor and carrier gases, the choice of precursors, the reaction chamber design, and the use of plasma enhancement during the deposition. These factors are discussed in the following sections.

4.1.2.1 Effect of Temperature during Atomic Layer Deposition

The ALD processing temperature, in particular the temperature of the substrate, is one of the key factors in ALD growth, with negative impact when the temperature is either too low or too high, as summarised in figure 4.6. When the processing temperature is low either i) the growth rate of the layer is reduced, as the precursors do not have sufficient thermal energy to react fully, or ii) the growth rate increases uncontrollably as precursors "condense" from the gaseous state on to the substrate without reacting, causing a quick building up of a thick layer of unreacted material. If the process temperature is high iii) the growth rate is reduced as precursors desorb from the substrate during the purge phase, leaving an incomplete monolayer for subsequent reactions, or iv) the precursors decompose on the substrate surface, preventing the layer by layer growth mechanism,

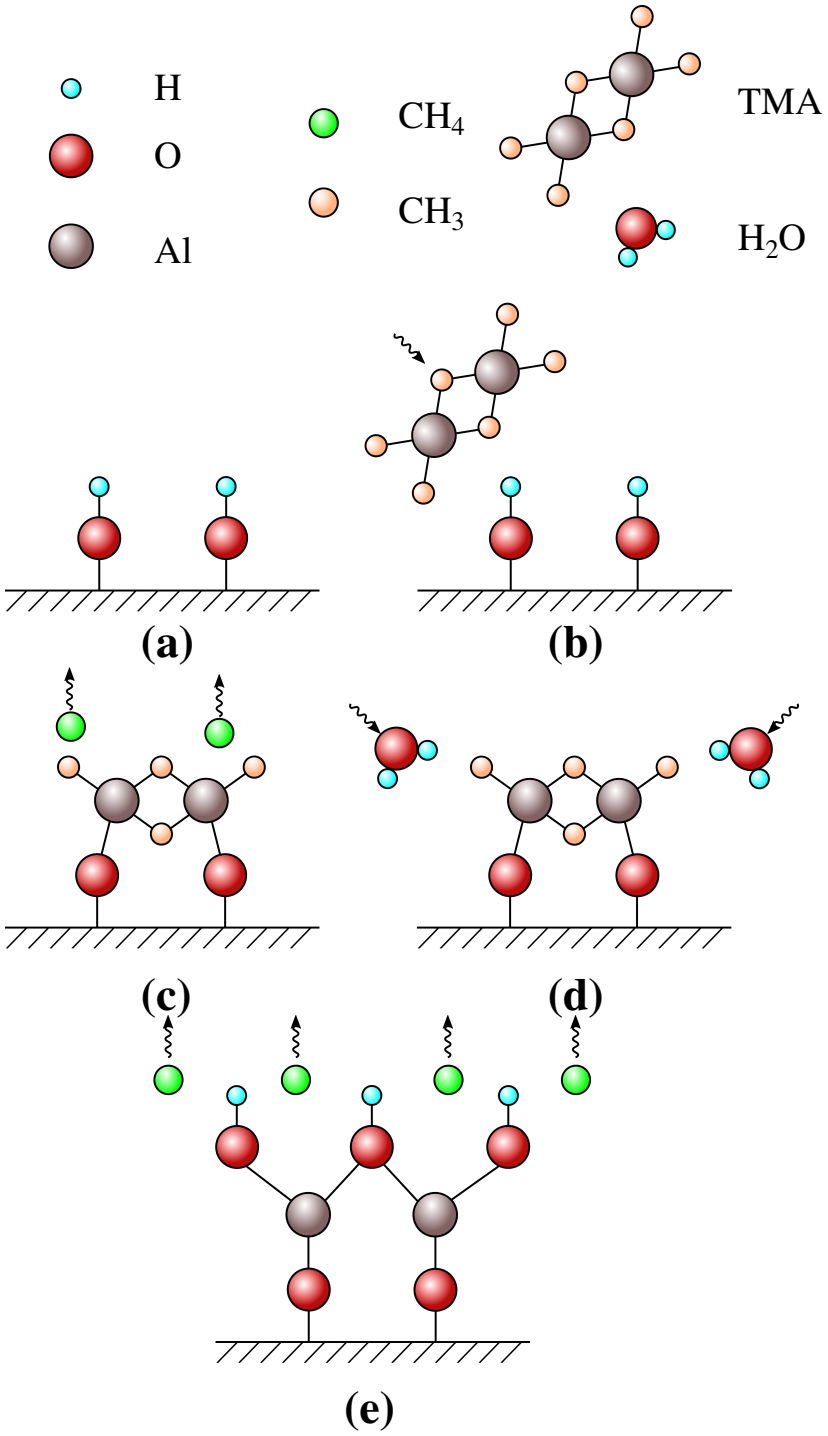


Figure 4.5: Illustration of the reaction mechanism used in ALD to build up monolayers of material, exemplified by the prototypical Trimethylaluminum (TMA) and water reaction to deposit aluminium oxide. **(a)** Hydroxyl groups saturate the sample surface. **(b)** TMA is introduced to the chamber. **(c)** One methyl group on the TMA reacts with the hydrogen from the hydroxyl group to produce a methane molecule, leaving the rest of the TMA molecule bound to the oxygen. The methane is removed by the purge gas. **(d)** Water vapour is introduced to the system. **(e)** One of the hydrogens in the water molecule bonds with one of the remaining methyl groups to produce methane, leaving a hydroxyl group terminating the surface. The produced methane is again removed by the purge gas. Steps **(a)** to **(e)** are repeated to build up the layers of Al_2O_3.

and leading to the build up of a thick layer of impure material.

These mechanisms typically leave a temperature range over which optimal deposition can occur, known as the ALD Process Window, during which time "ideal" ALD deposition is able to occur and the growth per cycle (GPC) should be constant. It should, however, be noted that observation shows that, particularly for metal oxides, GPC does reduce slightly over this process window [409]. For ALD of aluminium oxide from TMA and water this process window has been shown to be between around 180 °C and 250 °C [409], in which range all depositions took place throughout this work unless otherwise stated.

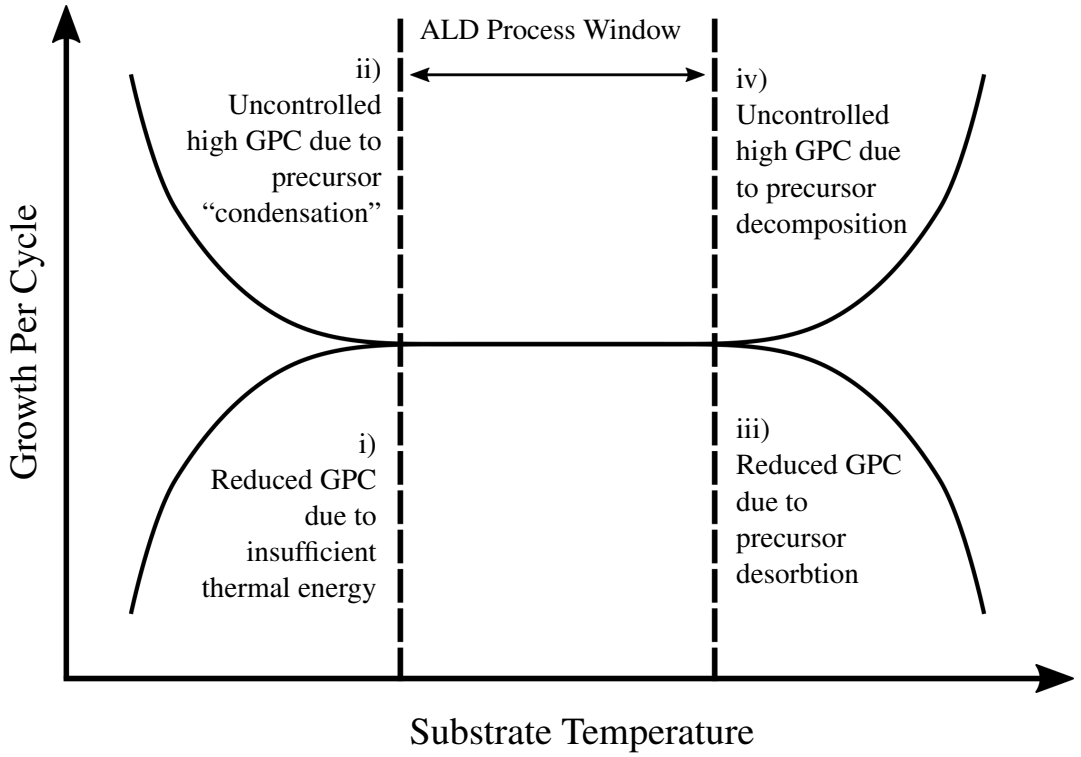


Figure 4.6: Illustration of growth per cycle (GPC) with temperature of the ALD process, demonstrating the ALD process window.

4.1.2.2 Control of Pulse and Purge Times for Precursors and Purge gases for Atomic Layer Deposition

The second set of highly significant parameters is the pulse/purge times of the precursor and carrier gases. These are the times for which the precursors are introduced to the reaction chamber, the pulse times (here t_{TMA} and t_{H_2O}), and the time allowed for the nitrogen stream to remove reaction by-products and excess precursors, the purge times (here $t_{P_{TMA}}$ and $t_{P_{H_2O}}$). The pulse times should be long enough to allow sufficient

precursor to enter the reaction chamber to saturate the surface of the substrate, occupying every available reaction site. However, this time must not be too long because, while the ALD reaction should be self limiting after a monolayer of precursor has been introduced, excess precursor may form a second incomplete layer, taking the deposition from the ALD regime into the Chemical Vapour Deposition (CVD) growth regime. Additionally, it is preferable to not introduce excess precursor as this increases the time needed for the subsequent purge step and is a waste of resources. Equally, purge times must be long enough to allow complete removal of excess material and reaction by-products, but will ideally be kept as short as possible in order to improve the deposition throughput and reduce the likelihood of precursor desorption during purging. Thus, similar to temperature, there is an optimal duration for t_{TMA}, t_{H_2O}, $t_{P_{TMA}}$, and $t_{P_{H_2O}}$. Figure 4.7 shows the expected GPC behaviour with the length of time for each step, which is dependent on species, chamber design, and temperatures.

4.1.2.3 Choice of Precursors for Atomic Layer Deposition

The choice, and purity, of the reagent materials (known as precursors) will also affect the ALD process. In particular, this will affect the quality and contamination of the layer deposited. Commonly there is a very limited range of precursors for a given material, so there is often little choice in precursor, although the purity varies depending on supplier. In this work the TMA precursor was produced by EpiValence, and is certified to contain less that 1 ppm of impurities. This was used since the quality of the gate insulator is critical in device performance. The second precursor was water that was obtained from a deionised water supply in house.

4.1.2.4 Plasma Enhancement for Atomic Layer Deposition

It is possible to enhance the deposition process through the use of a plasma, known as Plasma Enhanced ALD (PEALD). This has the advantage of reducing the necessary processing temperature, making it possible to even achieve optimal ALD growth at room temperature [411, 412], as well as facilitating the deposition of single elements (particularly metals), which cannot be processed by thermal ALD [410]. However, the plasma enhanced system has several major disadvantages. The system requires tight

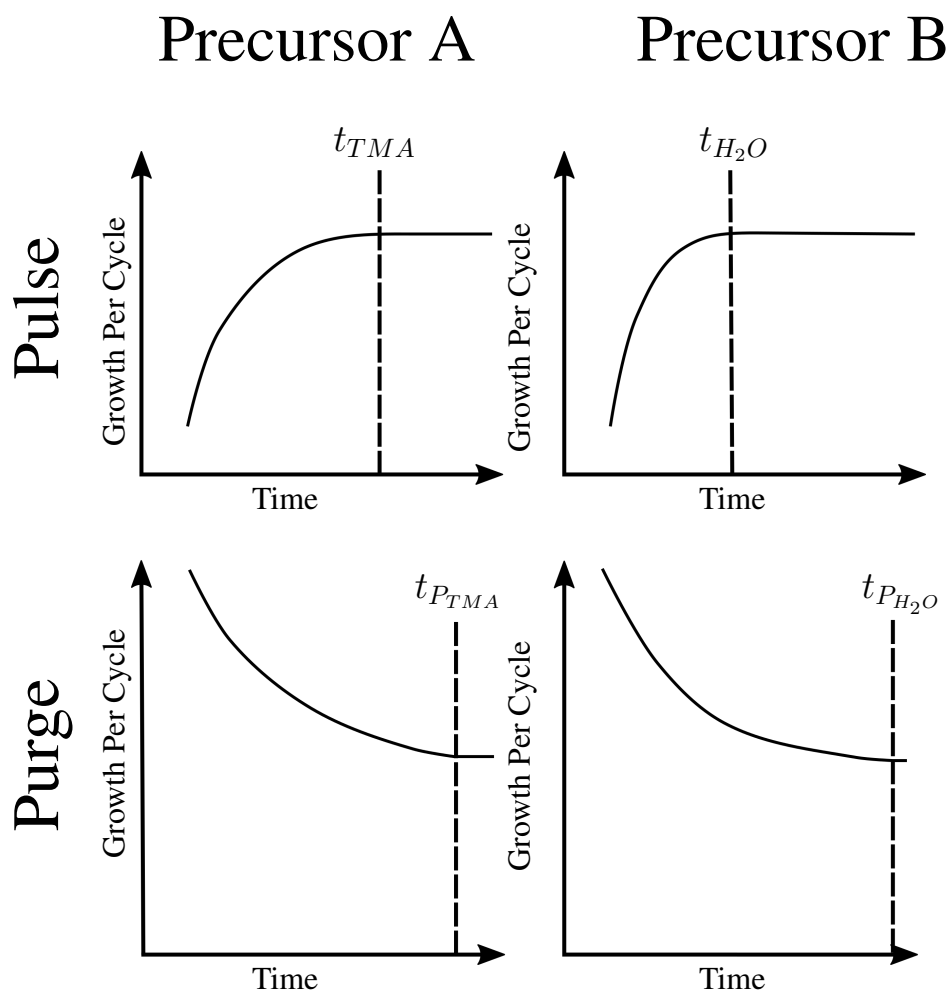


Figure 4.7: Schematic illsutration of ALD growth per cycle for the pulse and purge times for precursors in an ALD system. The optimum pulse and purge times are when the growth per cycle plateaus in each graph.

confinement of the plasma, using a field to prevent it from escaping and extinguishing, and exposure of the plasma to the surface of interest. This limits the chamber design to a single wafer chamber, greatly reducing the scope to increase throughput and production speed. A second limitation becomes apparent in the coating of samples with a high out-of-plane aspect ratio; here the coating becomes non-conformal across features due to the recombination of the plasma with the feature walls which reduces the plasma flux at the bottom of the feature, and leading to incomplete reaction of the precursors here [413]. More specific to this work, the use of a plasma has been shown to adversely affect the IGZO surface for the type of devices used in this work [414]. Therefore, only standard thermal ALD processes were considered.

4.1.2.5 Atomic Layer Deposition Reaction Chamber Design Considerations

A final consideration for the ALD process is the type and design of the reaction chamber. There are several options that have been demonstrated over the last twenty years, ranging from single wafer systems to large multi- (up to hundreds of) wafer systems, and even roll-to-roll systems.

There are two main design options: the traditional "temporal" ALD, where a precursor is introduced to the process chamber, the excess gas then purged, and the second precursor introduced, as described above, or the more recent "spatial" ALD, where the precursor gases are supplied continuously at the same time, separated spatially by a flow of the inert carrier gas, with the substrate moved between the precursor gases, see figure 4.8.

Spatial ALD is advantageous as it can greatly reduce the deposition time by avoiding evacuation of a large chamber during the purge phase, also it can operate under ambient atmospheric conditions and can be used for roll-to-roll processing in which a section of a roll of flexible substrate is run back and forth through the precursor gases to grow the desired thickness. This enables ALD deposition on a large substrate area, potentially kilometres at a time, without the need to load and unload substrates. A disadvantage of spatial ALD is that it either requires much more room (e.g. roll-to-roll systems), or can only process a single wafer at a time [164]. Spatial ALD is a relatively recent development [7, 415], and uncommon in commercial or academic settings.

Conversely, the maturity of temporal ALD means that such systems are far more common, making development work on them more accessible. For temporal ALD systems there are two main approaches: single wafer systems which are designed with a process chamber that fits the wafer very closely, thereby minimising purge and pulse times, reducing precursor waste, and allowing PEALD, and multiwafer (3D) batch systems, in which tens of wafers are processed simultaneously, greatly increasing the throughput, see figure 4.9. These approaches have positives and negatives, with the choice greatly dictated by the required throughput. In this work a 3D systems was used for all depositions. The tool used here was a Beneq TFS 500 fitted with a custom designed 3D chamber. The chamber used a horizontal design illustrated in figure 4.9**(b)**, as this produces gas flow very similar to that seen in the single wafer chamber depicted in figure 4.8**(a)**.

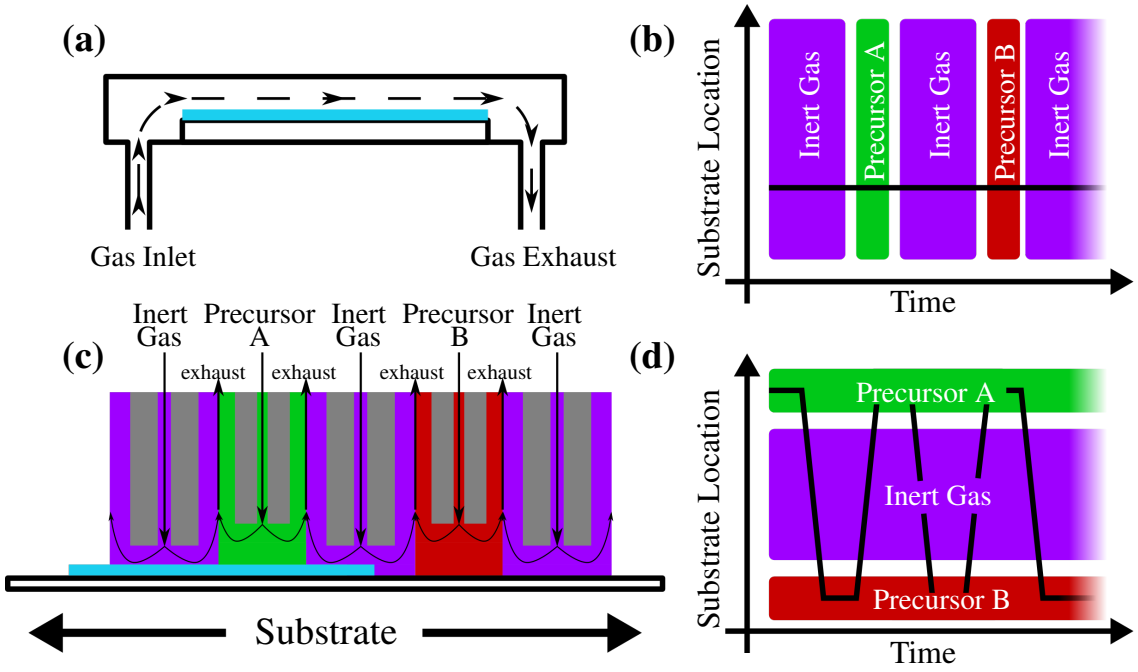


Figure 4.8: **a** and **c**, schematic representations of the gas flow in temporal and spatial ALD respectively. **b** and **d** the movement of the substrate with regard to the gasses. Adapted from Poodt et at. [415].

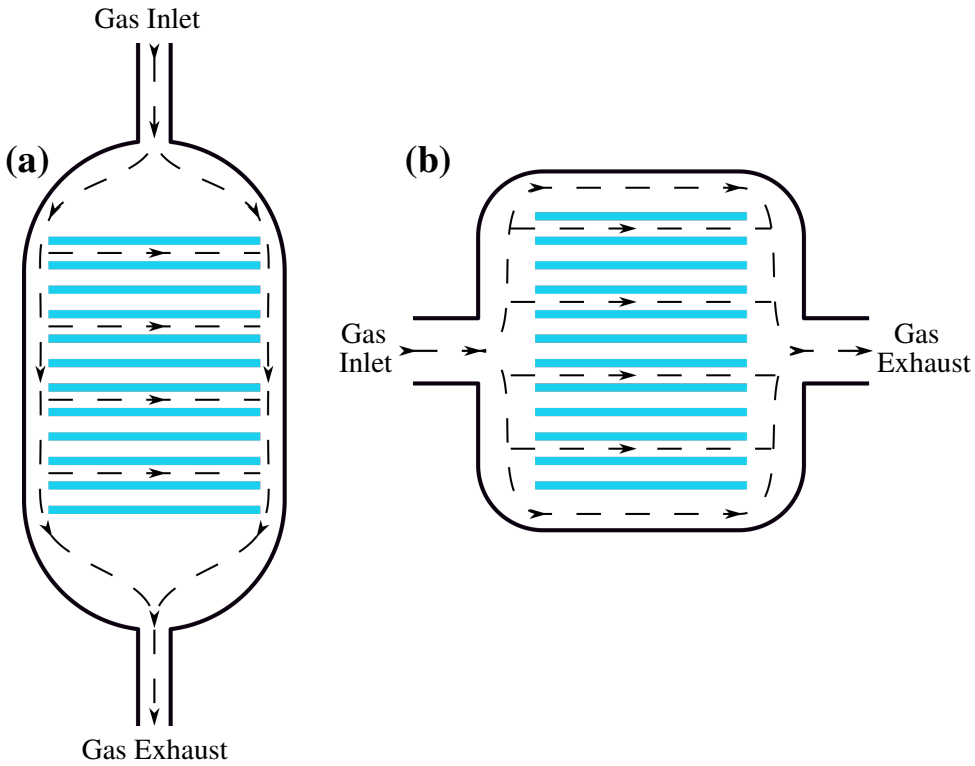


Figure 4.9: Schematic of the two main batch, or 3D, chamber designs used for temporal ALD. **(a)** is the more traditional vertical stack in which the precursor and purge gases diffuse across the wafers [416], **(b)** is the less common horizontal stack used in this work. The flow of precursor and purge gases is represented by the dashed lines.

4.2 Device Structure Definition

To take the deposited layers from simple stacks of material to functional devices, each layer must be patterned in some way to produce a 3D structure. There are multiple ways that this can be achieved, including standard photolithographic methods used throughout this work and discussed below, and other methods including electron or ion beam lithography, which provide very highly controlled patterning without the need for a mask, but at very much slower speed, or the more recently developed nano-imprint lithography which promises a route to commercial scale lithography of nanometre resolution features [417, 418].

4.2.1 Photolithography

Throughout this work, where structures are fabricated, the well established methods of photolithography are used. The process of photolithography involves the following steps, illustrated in figure 4.10:

1. Deposit material to be patterned
2. Deposit a layer of photoresist, usually through spin coating
3. Pattern photoresist by exposure to light through a mask
4. Develop photoresist to remove non-polymerised material
5. Etch deposited material where photoresist has been removed
6. Remove remaining photoresist

This process can be repeated for each layer to produce highly complex devices. The details of each step are largely determined by the material being patterned and the photoresist used.

4.2.1.1 Photoresists

A large range of photoresists exist, with different target applications, all of which work on the same principles. A uniform layer of photoresist, generally an organic monomer

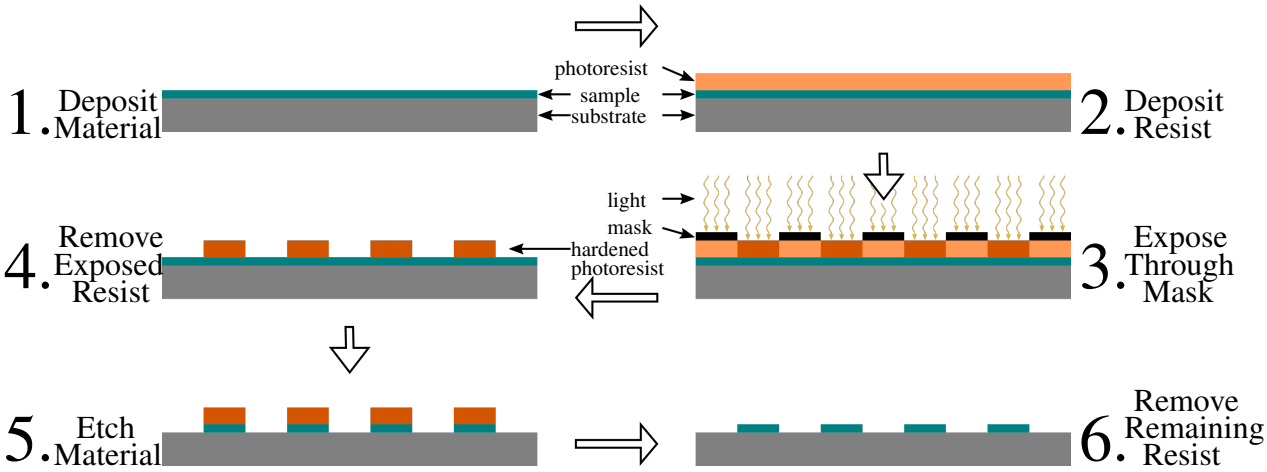


Figure 4.10: Illustration of the photolithographic process using a negative tone resist.

or polymer, is coated on the substrate. The substrate is then exposed to UV light in specific regions by exposure through a lithographic patterning mask. The exposure of the photoresist to light does one of two things: either the exposed region breaks down and becomes highly soluble in a solvent, called the developer. These photoresists are known as positive tone resists as the pattern of light exposed resist is removed. Alternatively, where the exposed regions become insoluble to the developer (either by polymerization of a monomer, or cross-linking between polymers) the unexposed regions dissolve in the developer; these resists are known as negative tone resists as the pattern transferred to the material is the opposite of the mask. When the substrate is then washed with the developer, the pattern defined by the mask is produced in the resist and through subsequent steps is patterned into the deposited material.

4.2.1.2 Patterning

After patterning the resist, the exposed regions of the deposited material are patterned by etching. This is either done through the use of acid or alkali etchant solutions, known as wet etching, or through plasma treatments known as dry etching.

Wet Etching

Wet etching is the use of acid or alkaline solutions to remove material through chemical reaction. A substrate is exposed to a suitable etchant, either by submerging in the solution or by spinning the wafer under a spray.

One prominent feature of wet etching is its isotropic nature when used with amorphous or nano-crystalline materials. That is, when a region is exposed to the etchant, the etching proceeds equally in all directions, such that etching extends laterally underneath the resist, see figure 4.11, known as undercut. Where precise control of dimensions is of high importance, this undercut can make wet etching a poor choice. In addition, the isotropic nature of the etching may be lost when single crystal, or poly-crystalline materials are used. Here the rate of etching may be dependent on crystal orientation and the presence of grain boundaries, such that anisotropy is introduced. There is, however, one significant advantage to wet etching: the selective nature of wet etching. Where multiple different materials are used in a fabrication process, the differing chemistries can be leveraged, and the etchants carefully chosen so that the etchant used for one layer does not etch the next layer and etching stops, at least in the out-of-plane direction, when the full layer thickness is reached.

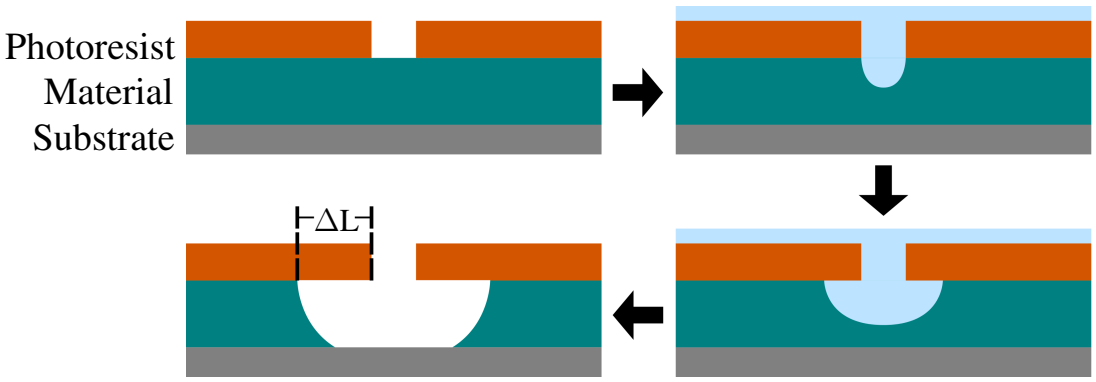


Figure 4.11: Undercut formation during wet etching. ΔL is the difference in feature dimensions between the mask design and the final pattern.

Dry Etching

Dry etching uses etchants in the plasma phase. This can be in the form of pure chemical etching, where a sample is exposed to a vapour of chemical etchants that work in much the same way as wet etching. Alternatively it can be reactive ion etching, where chemically reactive ions, such as fluorocarbons, oxygen, chlorine, etc., bombard the wafer, both reacting with the material, and physically dislodging it much like sputtering of a target during sputter deposition. Or finally pure physical etching, sputter etching, with ion bombardment being the only form of etching used.

Dry etching can be used in such as a way as to make it highly anisotropic, allowing production of features with high aspect ratios, while involving significantly less hazardous materials. This is particularly seen in sputter etching as there is no chemical reaction occurring. However, the lack of chemical reactivity significantly increases the time for such etching, and so reactive ion etching is often used as a compromise between throughput and directional selectivity. Even with the introduction of chemical etching, alongside the sputter etching, dry etching techniques suffer from lower throughput, requiring chambers to contain the plasmas at low pressure, and from a lack of material selectivity. This lack of selectivity extends not only to the different material layers in the stack, but also to the resist used to define the pattern since the dry etch process will attack the resist as well as the material that is deliberately being etched, albeit at different rates. This lack of selectivity must be considered when setting up the dry etch process, ensuring the resist is thick enough to protect the desired areas for the whole etching time, and that the etch does not go on longer that necessary for risk of etching the underlying layers.

Chapter 5

Measurement Techniques

Having prepared samples, several techniques were used for investigation of both material structure and functional electrical properties. In this work these included: X-ray reflectivity (XRR), X-ray photoelectron spectroscopy (XPS), surface energy measurements, and electrical transport measurements. These are described here with both theoretical discussion and experimental details. The following techniques are employed to give a detailed understanding of the structure of both individual material layers, and fabricated devices. Understanding of these structures is key to improving device performance and so these techniques are of great importance.

5.1 X-ray Reflectivity (XRR)

Grazing incidence X-ray Reflectivity (XRR) is a non-destructive technique for the investigation of thin-film structures. XRR measurements yield information on film thickness, density and surface/interface widths in films of single- or multi-layered materials in a stack. An overview of the technique and a discussion of how results can be extracted from the data using the GenX software package are presented here.

5.1.1 Overview of X-ray Reflectivity

There are many published works on the theory of XRR, for example [419] and [420] which may be referred to for further information. XRR is based on the interactions between X-rays and electrons, where elastic, or Thomson, scattering takes place.

Scattering is weak, so only one scattering event per wave need be considered. In addition, the Fraunhofer far-field approximation is assumed to hold, such that X-ray detection happens far enough from the sample that scattered waves can be considered parallel at the detector.

5.1.2 Reflections from a single interface

X-ray scattering at a surface results in both reflection and transmission of the beam, see figure 5.1, where the reflection angle, α_r, and the transmission angle, α_t, depend on the incident angle, α_i, and the refractive indices of the materials, n_0 and n_1. n is governed by the electron density in the material as:

$$n = 1 - \delta + i\beta \tag{5.1.1}$$

where δ is the dispersion coefficient and β is the absorption coefficient.

The propagation of the reflected and transmitted beams is governed by Snell's law and the Fresnel equations (which can be derived from the continuity of waves and their derivatives over the interface) [421, 422]. Total external reflection occurs when the real part of the transmitted beam diminishes to α_t = 0. For small α_i, Snell's law,

$$n_0 \cos(\alpha_i) = n_1 \cos(\alpha_t) \tag{5.1.2}$$

can be reduced to give the critical angle, α_c:

$$\alpha_c = \sqrt{2(1 - n_1)} = \sqrt{2\delta} \tag{5.1.3}$$

where δ is the dispersion factor from above. The Fresnel equations for reflectivity, r, and transmission, t, describe how the waves travel between layers of different refractive

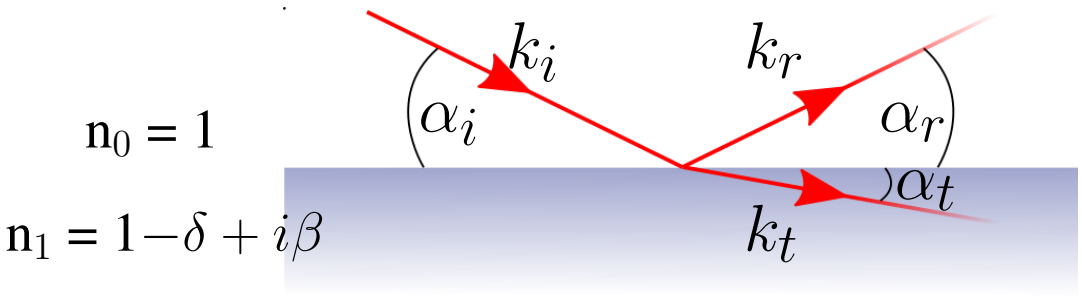


Figure 5.1: Reflection of X-rays from a single infinitely thick slab of material

indexes. In angular terms these are given as:

$$r = \frac{n_0\alpha_{i,r} - n_1\alpha_t}{n_0\alpha_{i,r} + n_1\alpha_t} \tag{5.1.4}$$

$$t = \frac{2n_0\alpha_{i,r}}{n_0\alpha_{i,r} + n_1\alpha_t} \tag{5.1.5}$$

The measurable intensity from reflection and transmission are then $R = |r|^2$ and $T = |t|^2$. Below the critical angle only R exists, above it transmission increases and reflectivity drops as α_i^{-4}, leading to a characteristic slope as shown in figure 5.2.

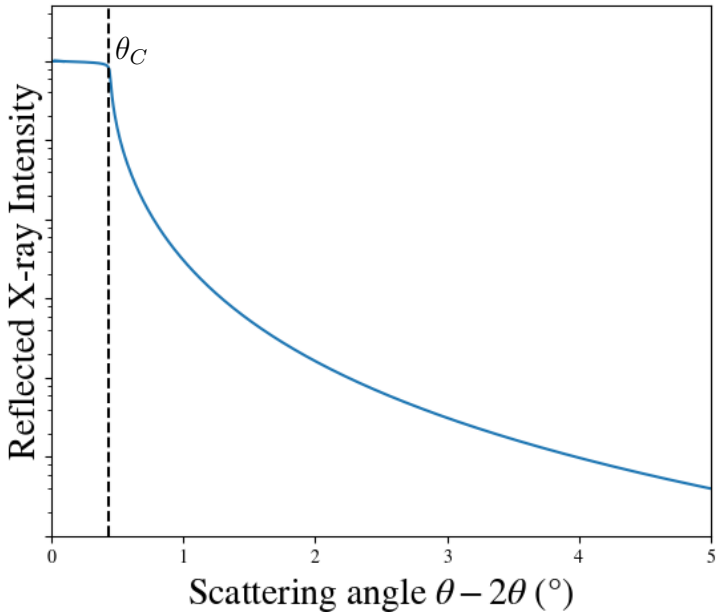


Figure 5.2: Simulation of the characteristic X-ray reflectivity from a single, infinitely thick, slab of silicon

5.1.3 X-ray Reflectivity from a thin-film

The Fresnel equations for r and t refer specifically to a single interface between two infinitely thick materials. However, in thin-films below around 100 nm, there are two interfaces, the top and the bottom interface. Both of these interfaces obey Snell's law and the Fresnel equations, meaning there are successive bounces of transmitted and reflected beams, illustrated in figure 5.3, which must be summed together following the method of

Als-Nielsen [423, 424], to get the Fresnell reflectivity:

$$r_{slab} = r_{01} + \frac{t_{01}r_{12}t_{10}p^2}{1 - r_{10}r_{12}p^2} = \frac{r_{01} + r_{12}p^2}{1 + r_{10}r_{12}p^2} \tag{5.1.6}$$

where p is the phase factor accounting for the path difference as $p^2 = \exp(iqd)$ where d is the thickness of the layer, $q = 2k_1 \sin(\alpha_1)$ and k_1 is the incident wavevector.

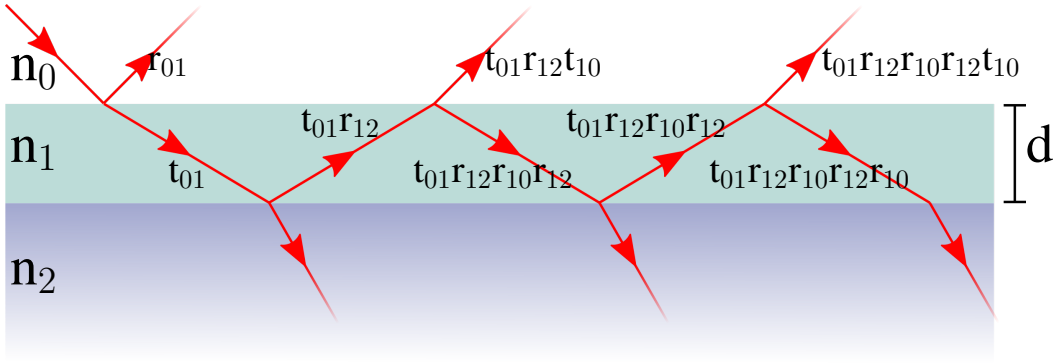


Figure 5.3: Schematic illustration of the reflection of X-rays from a single thin-film on top of an infinitely thick slab of material, the critical angle α_c is marked as $2\theta_c$.

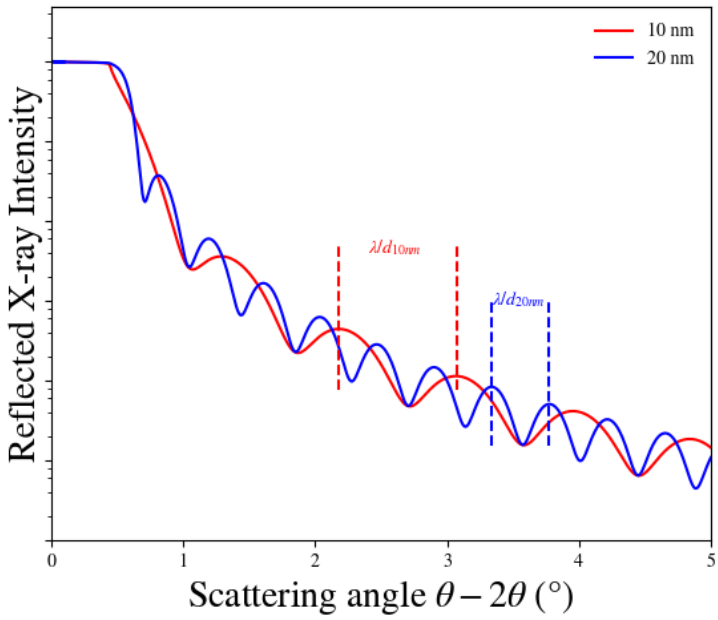


Figure 5.4: Simulations of X-ray reflectivity from smooth thin-films of aluminium oxide on an infinitely thick silicon substrate. The spacing of the Keissig fringes gives information about the thickness of the films.

5.1.4 Reflections from multiple thin-films

This formalism can be further extended to many layers of material in a stack following Parratt's recursive method [425] to give the reflectivity from the top of each layer accounting for all the layers below it as

$$r_{j-2,j-1} = \frac{r_{j-2,j-1} + r_{j-1,j}p_{j-1}^2}{1 + r_{j-2,j-1}r_{j-1,j}p_{j-1}^2} \tag{5.1.7}$$

where j refers to each layer, with refractive index n_j and thickness d_j. This formula is applied recursively, starting with the substrate interface, through to the top interface to determine $r_{0,1}$. Figure 5.4 shows an example of the specular reflectivity, $R = |r|^2$, as a function of the incident X-ray angle for two thin aluminium oxide films on an infinite Si substrate, with aluminium oxide films with thickness of 10 nm and 20 nm. The α_i^{-4} trend in intensity remains, but with interference fringes, known as Kiessig fringes, superimposed [426]. The Kiessig fringes reach maxima when the phase factor, $p^2 = \exp(idq)$, between the reflected waves from the top and the bottom interfaces of the film, thickness d, results in constructive interference. i.e. when:

$$d\sin(\alpha t) = m\lambda \tag{5.1.8}$$

where m is an integer and λ is the X-ray wavelength. From this, with small incidence and critical angles, the angular difference between two consecutive fringes, m and $m+1$, is:

$$\alpha_{m+1} - \alpha_m = \frac{\lambda}{d} \tag{5.1.9}$$

5.1.5 Reflections from a rough interface

So far only perfectly smooth, sharp interfaces have been considered. In practice interfaces have some finite width due to topological roughness and chemical intermixing, with a width σ, see figure 5.5. Specular reflectivity cannot differentiate between these two types of intermixing, as both contribute to σ. This interface can be represented by a series of flat surfaces described by a Gaussian with a standard deviation σ. The reflectivity of this interface can then be found as the reflected contribution from each of these layers, integrated over the interface width in the z direction, with a density profile described by an error function, $erf(z) = \sqrt{2\sigma}$, and with a change of phase from each component

$p^2 = \exp(iqz)$. The total reflectivity from the interface then becomes:

$$R = R_{smooth} \exp\left(-q^2\sigma^2\right) \tag{5.1.10}$$

and its effect is illustrated in figure 5.6. A complementary technique to specular X-ray reflectivity, transverse diffuse scattering measurements, can be used to distinguish between the intermixing roughness and topological roughness, as detailed below.

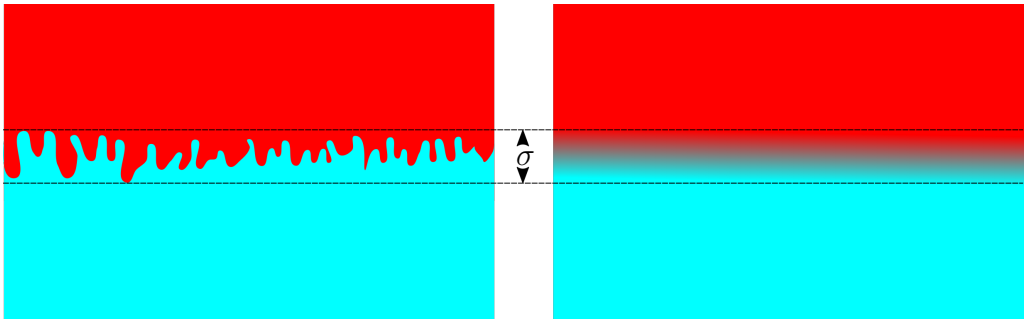


Figure 5.5: Schematic illustration of two possible interface types, both of which contribute to the interface width. Both examples have the same interface width, σ, left demonstrates topological roughness, while right is chemical intermixing.

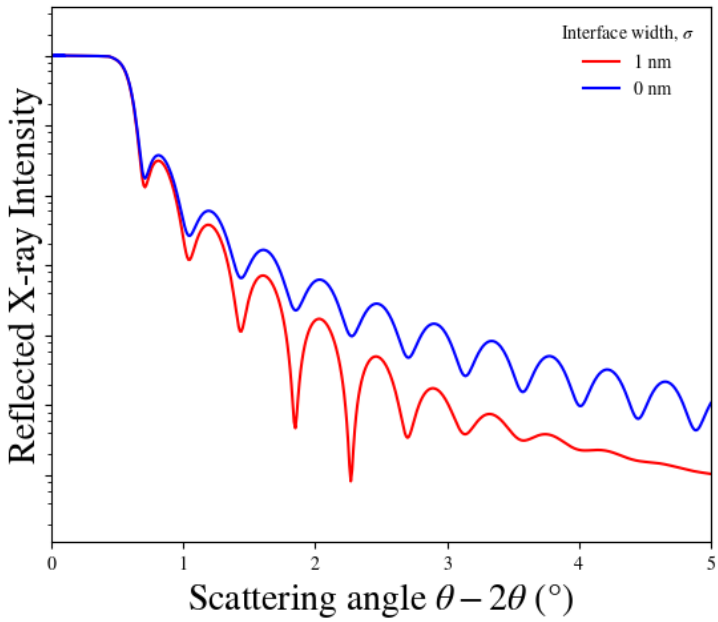


Figure 5.6: Simulations of reflectivity from thin-films of alumina on an infinitely thick silicon substrate with differing interface widths. Increasing the interface width causes the Keissig fringes to be lost at higher angles.

5.1.6 Diffuse Scatter

As discussed above, the intensity of the reflected beam at the angle $\alpha_r = \alpha_i$ is governed by equation 5.1.10. However, there is a portion of the incident beam which is reflected at $\alpha_r \neq \alpha_i$, known as diffuse scattering, and is caused by the topological roughness at the interface. Where the interface between layers is smooth there is little or no diffuse scatter, but where the interface is rough, diffuse scatter can be significant.

5.1.6.1 Forward Diffuse Scattering

In the forward direction this diffuse scattering can contribute to the measured specular scatter, distorting results. To remove any diffuse scatter a second measurement should be performed, offset from the specular ridge (where $\alpha_r = \alpha_i$) by a small amount, and then subtracted from the specular measurement before fitting [427]. In this work the offset of the diffuse scan is 0.2°. Forward diffuse scans were performed for the initial measurement of each sample, and where forward diffuse scatter was found to make a significant contribution to sample analysis it was repeated for all specular scans.

5.1.7 Transverse Diffuse Scans

In the transverse direction this diffuse scattering can be utilised to examine the distinction between topological roughness and chemical intermixing at the interface, figure 5.5. For a transverse diffuse measurement, also referred to as a Rocking Curve (similar to rocking curves in X-ray diffraction), the detector angle is fixed and the sample scanned, or rocked, over the specimen's rotation axes, see figure 5.7. The signal measured from such scans is determined by the fundamental properties of the material and diffuse scatter from roughness at the interfaces of the sample. Such data can be fitted to a model based on the distorted-wave Born approximation (DWBA) developed by Sinha, Sirota, Garoff, and Stanley [428], and further extended by Wormington et al. [427]. This takes account of the contributions to the interface from topological roughness and chemical intermixing. Sinha et al. give a full analytical description of the specular reflectivity [428] which describes topological roughness at the interface, while Worminton et al. add a further term to describe chemical intermixing [427]. Of note from these works is the autocorrelation

term, $C(X)$, describing interface topology put forward by Singha et al.,

$$C(X) = \langle \eta(0)\eta(X) \rangle = \sigma^2 \exp\left(- \left| \frac{X}{\xi} \right|^{2H} \right) \tag{5.1.11}$$

where $\eta(0)$ is the centre of the measurement area, $\eta(X)$ is some random other position within the measurement, and $\langle \cdots \rangle$ represents an average over the whole measurement area. On the right hand side of the equation σ is the total interface width, X is the separation of points within the measurement area, ξ is the correlation length, and H is the Hurst parameter describing the jaggedness of an interface [428]. While equation 5.1.11 describes the autocorrelation in just one layer, this was later expanded by Ming et al. [429] and Tolan et al. [430] to include multiple layers as

$$C(X) = \sigma_i \sigma_j \exp\left(- \left| \frac{X}{\xi} \right|^{2H} \right) \exp\left(\frac{-|\Delta z_{i,j}|}{\xi_\perp} \right) \tag{5.1.12}$$

where i and j refer to the respective layers, $\Delta z_{i,j}$ is the distance between layers, ξ remains the in-plane correlation length, and $\xi_\perp$ is the out-of-plane correlation length.

The above autocorrelation function means there are several parameters found when fitting such transverse diffuse scans, namely ξ, $\xi_\perp$, and H which are described again when results are presented. It should be noted that the use of this extended DWBA model required significant computational power when fitting, which has lead many previous works to fit such scans in a semi-manual way, rather than using computational algorithms, or simply to using the ratio of the specular peak to the off-specular background to estimate the relative contributions of intermixing and roughness [420,431] . With the increasing computational power available, and particularly with the use of cluster systems, it has been possible here to employ the GenX genetic fitting algorithm to fit both the specular and transverse scans simultaneously, even for multiple transverse scans, yielding an understanding of the interface that would otherwise have not been possible.

With a single interface between a thin-film and substrate, a single transverse scan is sufficient to accurately model that interface. However, with more interfaces it is necessary to take scans at the maxima of successive Kiessig fringes to inform on interfaces.

In this work transverse scans were taken at the first two Kiessig maxima, figure 5.7.

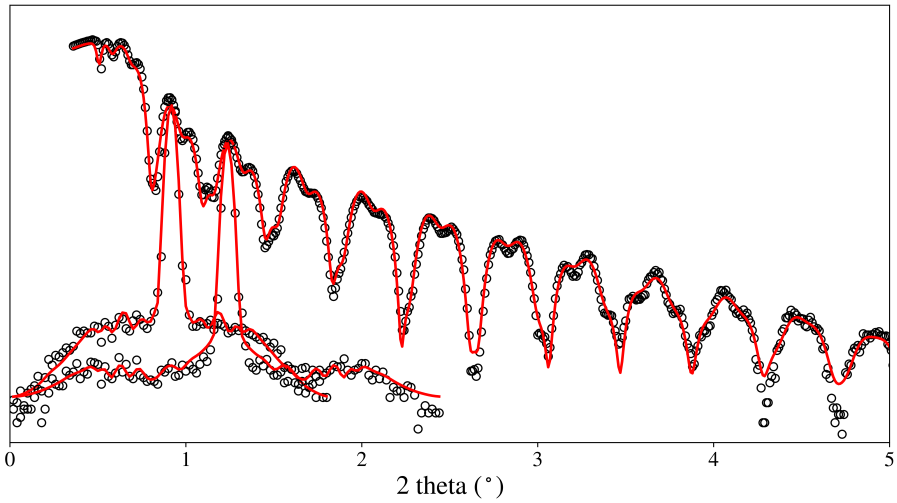


Figure 5.7: Example of transverse diffuse scans, data in black circles, performed on a sample of ALD Al_2O_3 on a-IGZO, deposited on silicon. The best fitting model found using GenX is shown in red with good agreement between the measured data and the model. The transverse scans are projected onto the 2θ axis for viewing.

5.1.8 Experimental Detail for X-ray Reflectivity

All XRR data used throughout this study was captured on a Bede D1 High Resolution Diffractometer equipped with a copper X-ray source, and aligned to select just the Cu-Kα_1 characteristic X-ray line using a double bounce channel cut silicon crystal. See figure 5.8. Here the angle between the X-ray beam and the sample, the incident angle referred to as α_i above, is now referred to as θ. Specular measurements are taken (when $\alpha_r = \alpha_i$) by coupling the movement of the detector to that of the sample relative to the beam. As such the detector moves from the straight through orientation, by twice the rotation of the sample, and this angle is referred to as 2θ. Specular reflectivity scans were performed for 2θ values between 0° and 5° with 0.1° steps, and count times of 3 seconds per point. Forward diffuse scans were performed with the same set up but with a 0.2° offset of the θ axis. Transverse scans were taken by holding the detector at an angle of 2θ slightly above the critical angle, and rotating the sample around its axis from 0° and $2\theta^\circ$ with 0.1° steps and 6 second count times.

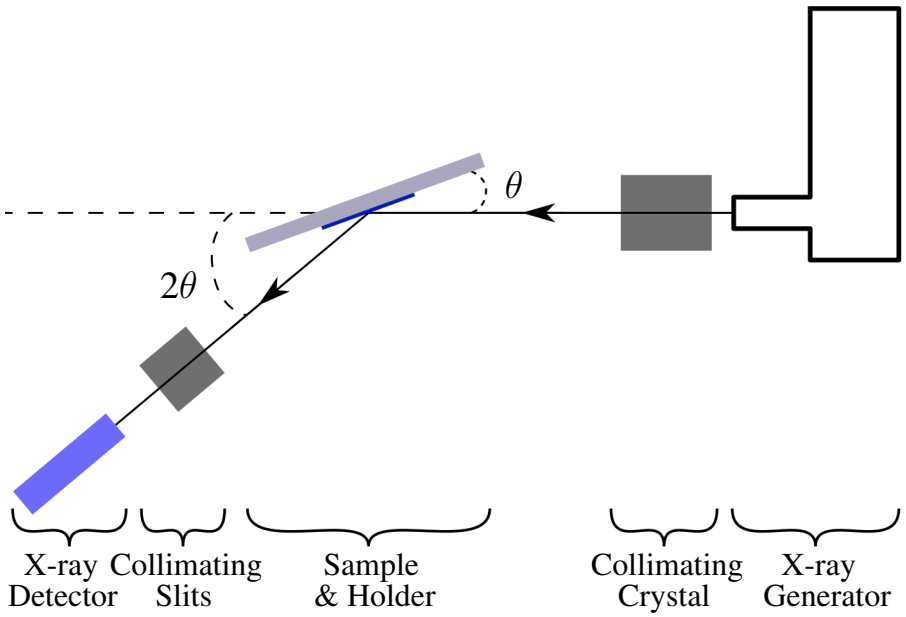


Figure 5.8: Schematic of the Bede D1 High Resolution Diffractometer. For standard specular scans θ and 2θ motors are linked.

5.1.8.1 X-ray Reflectivity data fitting using a genetic algorithm in the GenX software package

The extraction of information from XRR data relies heavily on computer power to generate and test the *goodness of fit* of physical simulations. GenX, an open source, free to use, and highly versatile software package was used here [432]. GenX uses differential evolution, a form of genetic algorithm, to fit a model system to the data [433] by varying the physical model parameters and choosing the resultant simulations with the smallest Figure of Merit (FOM) to move forward to the next generation. By varying the free parameters over progressively smaller ranges, GenX is able to fit multiple parameters at once for highly complex layer stacks. For a detailed guide to using GenX for XRR fitting see the work of Inyang [434]. Two factors influence the outcome of this fitting process: the starting model system, and the FOM. The starting model is important as a starting point close to the final answer greatly reduces the likelihood of the fitting process converging to a local minimum, as opposed to the true global minimum, FOM value. While convergence to a local minimum is unlikely in simple systems, such as single layer films, in which only a very few free parameters exist, it becomes more likely as the complexity of the system increases. Given this dependence on the initial model, it is necessary to inspect fits to make sure the fitted model truly resembles the acquired data,

and where it does not, a new model may be needed. Throughout this work, the model used for each material is discussed alongside results.

The GenX Figure of Merit (FOM)

One of the key factors in achieving a good fit of the model system to the measured XRR data is the way the fit is evaluated. In GenX this is assessed using the Figure of Merit (FOM), where a better fit is indicated by a lower value of the FOM. The standard approach to model fitting is a chi squared (χ^2) minimisation [435], in which the error weighted difference between each measured data point and the corresponding model point is summed. However, χ^2 minimisation is an inappropriate tool where data spans many orders of magnitude in the y-axis, as with XRR data (data in the work spans around 6 orders of magnitude). GenX does provide other FOMs that can be used, from the simple difference between the model and measured values, to more XRR specific FOMs such as Sintth4, which weights the difference by $\sin(2\theta)^4$ to account for the Fresnel reflectivity described in section 5.1.2. There are also FOMs that take account of the error on each measured data point, normally taken as the Poisson error, such as the χ^2 method described above. Far more detail of these FOMs can be found in the built-in GenX documentation.

These FOMs all have limitations which make them less than satisfactory for this work where fitting of both the low angle data (dominated by signal from the top layer) and higher angle data (dominated by signal from the lower layers, and containing vital information about interface widths) is of great importance. In addition, the inbuilt FOMs provide no means by which the focus of the fitting can be altered by the user - a particular problem when higher angle data is particularly noisy (see for example the fitting of aluminium oxide layers in chapter 7), where these FOMs cause the program to try and fit to data with little or no physical meaning.

To overcome these limitations a custom written FOM was used in this work. This FOM is derived from the supplied log and $logbars$ FOMs (FOM$_{log}$ and FOM$_{logbars}$) respectively). FOM$_{log}$ takes the average absolute difference in the $\log_{10}$ of the measured and simulated data, while FOM$_{logbars}$ does the same and then weights each data point by $E_i \ln(10) N_i$, where N_i is the data point and E_i is the error on that point supplied along with the data.

While these methods avoid the strong influence of the high count (low angle) data, FOM_{log} gives no consideration of the errors, and $\text{FOM}_{logbars}$ requires the user to supply the error on each data point externally (not normally a data set supplied by XRR apparatus) and also distorts this weighting by the additional $\ln(10)$ term.

In this new FOM, the average absolute difference in the data and simulation are still used, but they are now weighted instead by the Poisson counting error on each point ($\sqrt{N_i}$) and a user controlled constant, n. This is then described as

$$FOM = \frac{1}{N-p}\sum_i \frac{|\log_{10}(N_i) - \log_{10}(S_i)|}{\log_{10}(\sqrt{N_i}+n) \times \log_{10}(N_i)} \tag{5.1.13}$$

where N is the total number of data points, p is the number of free variables in the fit, N is the input data set, S is the simulated data set, and i is an individual element within these data sets. Finally, n is an additional weighting term which can be used to shift the focus away from the higher angle noisy data. This new FOM not only produced superior fitting in practice, but also has a more thorough grounding in the management of expected errors on counting type errors (i.e. Poisson errors) as described well by Hughes & Hase [435].

A final note on this new FOM is that, as the error on the data is assessed as $\sqrt{N_i}$ for all data points, it is only appropriate for use where the data is collected for a set count time at each point. However, where data is collected with a variable count time to achieve a set count (C), this could be replaced with $N_i/\sqrt{C}$.

Density in GenX

One important point to note with GenX fitting is with regards to the material density. The density is calculated in GenX as the scattering length density (the X-ray scattering length multiplied by the density). Therefore, how the scattering length is defined and scaled is very important in calculating the density. GenX has several in built scattering length databases, of which fp and fw, from Henke [436] are appropriate for XRR. fp has units of electrons (or rather Thomson scattering lengths), meaning that any densities fitted for a layer using fp, is in formula units per cubic angstrom (u/Å^3). If one uses fw, the scattering length of an atom has been scaled by its atomic weight. Consequently the density can be inserted in units of g/cm^3. However fw then requires that the materials composition must be given in weight percent of each element, whereas fp allows the chemical composition

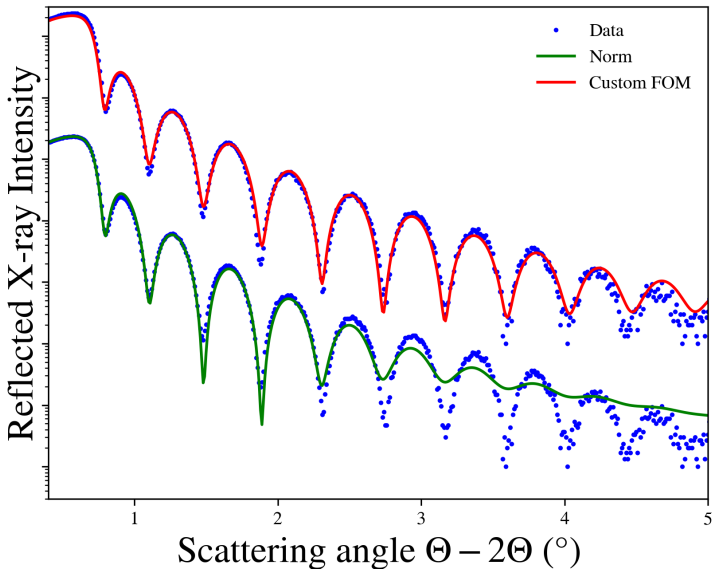


Figure 5.9: XRR fitting for a ∼20 nm film of IGZO using the Norm FOM and the custom FOM defined by equation 5.1.13. Norm FOM fits the low angle, high intensity data well, but loses accuracy as the intensity drops, where as the custom FOM fits all of the data well. Data is arbitrarily offset for easy of viewing.

to be entered, therefore fp was used here. The film density can then be converted from the scattering length density to mass density as

$$\rho_{mass} = \frac{\rho_{GenX}}{1.66054 \times 10^3 \times u_{scatt}} \tag{5.1.14}$$

where ρ_{mass} is the material density in g/cm^3, ρ_{GenX} is the material density in formula units per Å^3 calculated in GenX, and u_{scatt} is the molecular weight of one formula unit

$$u_{scatt} = \sum_i u_i \times x_i \tag{5.1.15}$$

where u_i is the weight of each constituent atom in relative atomic mass, and x_i is the number of those atoms in each formula unit [437].

5.2 X-ray Photoelectron Spectroscopy

X-ray photoelectron spectroscopy (XPS) is an X-ray technique harnessing the photoelectric effect to identify chemical composition of a sample [438]. The premise of the technique is that monochromated X-rays illuminate the sample surface, exciting electrons in the surface layers so that they are emitted from their atoms. The kinetic

energy, E_{KE} of these atoms is then measured using a spectrometer, and the energy that was binding the electron to the atom, $E_{binding}$, is calculated as

$$E_{binding} = hf - E_{KE} - \phi \tag{5.2.16}$$

where h is Plank's constant, f is the frequency of the X-rays (so hf is the energy of the X-rays), and ϕ is the work function between the sample and the instrument (established by reference to measurements of known materials).

The intensity of electrons across the energy spectrum is measured, with characteristic peaks appearing at energies corresponding to the energy levels of elements in the sample. As all elements have different spectra, these peaks are used as a "finger print" allowing the chemical composition to be calculated, while the relative intensity of each peak is used to calculate the ratio of constituent atoms. In-depth coverage of XPS is available in works from Watts & Wolstenolme, and Seah & Briggs [439, 440].

In this work, all XPS measurements and analysis were carried out by Kratos Analytical Ltd. using an AXIS Nova spectrometer.

5.3 Contact Angle and Surface Energy

Contact angle measurements are predominately used to investigate the wettability of a solid surface by a particular liquid. However, through the use of multiple liquids, it can be used to investigate the surface energy of a solid surface. This is know as the sessile drop technique. The contact angle is a measure of the angle of a liquid droplet at the liquid-vapour interface, figure 5.10. This is measured by taking an image of the droplet from an in-plane angle, and either directly measuring the angle or fitting the Young-Laplace equation to the droplet and extracting the angle using the Young equation [441] as

$$\gamma_{SG} - \gamma_{SL} - \gamma_{LG} \cos\theta_C = 0 \tag{5.3.17}$$

where γ_{SG} ,γ_{SL} ,γ_{LG} refer to the interfacial energies at the Solid-Gas, Solid-Liquid, and Liquid-Gas interfaces respectively, and θ_C is the contact angle [442].

To calculate the surface energy the Owens, Wendt, Rabel, and Kaelble method is used.

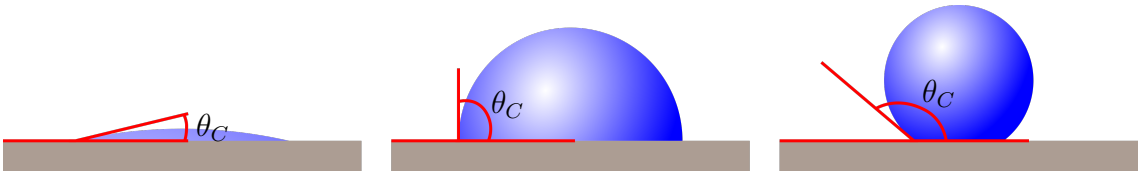


Figure 5.10: Contact angle for liquids with different levels of hydrophilicity

This method takes Young's equation and uses Fowkes' assertion that γ_{SL} is the geometric mean of two components, a dispersive part and a polar part, such that

$$\gamma_{SL} = \gamma_{SG} + \gamma_{LG} - 2(\sqrt{\gamma^D_{SG} \cdot \gamma^D_{LG}} + \sqrt{\gamma^P_{SG} \cdot \gamma^P_{LG}}) \tag{5.3.18}$$

where γ^D is the dispersive component and γ^P is the polar component [443], to give [444]

$$\frac{(1 + \cos\theta_C)\,\gamma_{LG}}{2\sqrt{\gamma^D_{LG}}} = \frac{\sqrt{\gamma^P_{SG}}\sqrt{\gamma^P_{LG}}}{\sqrt{\gamma^D_{LG}}} + \sqrt{\gamma^D_{SG}}\,. \tag{5.3.19}$$

If this is viewed in the form of a general linear equation, $y = mx + c$, then an unknown solid surface energy, γ_{SL}, can be calculated from a graph of the contact angles for two or more liquids of known γ^P_{LG} and γ^D_{LG}, with the form

$$y = \frac{(1 + \cos\theta_C)\,\gamma_{LG}}{2\sqrt{\gamma^D_{LG}}}\ ;\ m = \sqrt{\gamma^P_{SG}}\ ;\ x = \frac{\sqrt{\gamma^P_{LG}}}{\sqrt{\gamma^D_{LG}}}\ ;\ c = \sqrt{\gamma^D_{SG}} \tag{5.3.20}$$

In order to simplify this further, generally one liquid with zero polar component and a known dispersive component, and one liquid with both a known polar and known dispersive components are used. In this work diiodomethane ($\gamma^P_{LG} = 0, \gamma^D_{LG} = 50.8$) [445] and high purity water ($\gamma^P_{LG} = 51.5, \gamma^D_{LG} = 21.8$) [446] are used as the two liquids.
The measurements are performed on a contact angle rig with a channel surrounding the sample and a cover to create a saturated ambient gas environment to reduce evaporation. A droplet of liquid (2 μL of water, 0.5 μL of di-i-odomethane) is dispensed onto a clean area of the sample and images captured every second for 30 seconds. The Young-Laplace curve is then fitted to the images and the average contact angle found from both sides of the droplet. This is repeated 9 times for each liquid and the angles used, as described above, to calculate the dispersive and polar components of the sample after removal of outlying measurements caused by sample contamination.

5.4 Electrical Transport Measurements

One of the objectives of this work is to link the materials properties, as measured through the techniques described earlier in this chapter, to device performance and electrical parameters. As such it is important that reliable and comparable device measurements are made that allow key electrical performance indicators (KPIs) to be compared and their relation to material properties properly understood. The methodology for extracting KPIs is described below, having previously discussed their theoretical basis in chapter 2. Some of these KPIs are expected to be the same regardless of device design variations, but others are dependent on factors such as the semiconductor channel length and width, and so, where KPIs are discussed, the channel lengths and widths are also included to allow accurate comparisons.

All measurements were made using an 18 channel probe station, made up of 18 Keithley 2612 series source measure units (SMUs), with a custom designed probe card to perform on-wafer device testing, and carried out by technicians at Pragmatic Printing Ltd.

5.4.1 Current-Voltage Sweeps

Current-Voltage measurements, or IV sweeps, were performed between -6 V and 6 V, with the device drain bias set at 1 V and the source bias at 0 V. A step size of 0.025 V is used between -2 V and 2 V, and 0.25 V outside this range, facilitating more accurate extraction of KPIs from around the transition region. Each step has a 70 ms dwell time to allow the measurement to stabilise. The sweeps were performed in both the positive (-6 V to 6 V) and negative (6 V to -6 V) directions.

5.4.2 KPIs

The physical meaning and origin of these KPIs is discussed in detail in chapter 2, so here are given details of how these data are extracted from the IV sweeps discussed above. Figure 5.11 shows an IV curve representative of those seen in this work, with the extracted KPIs indicated.

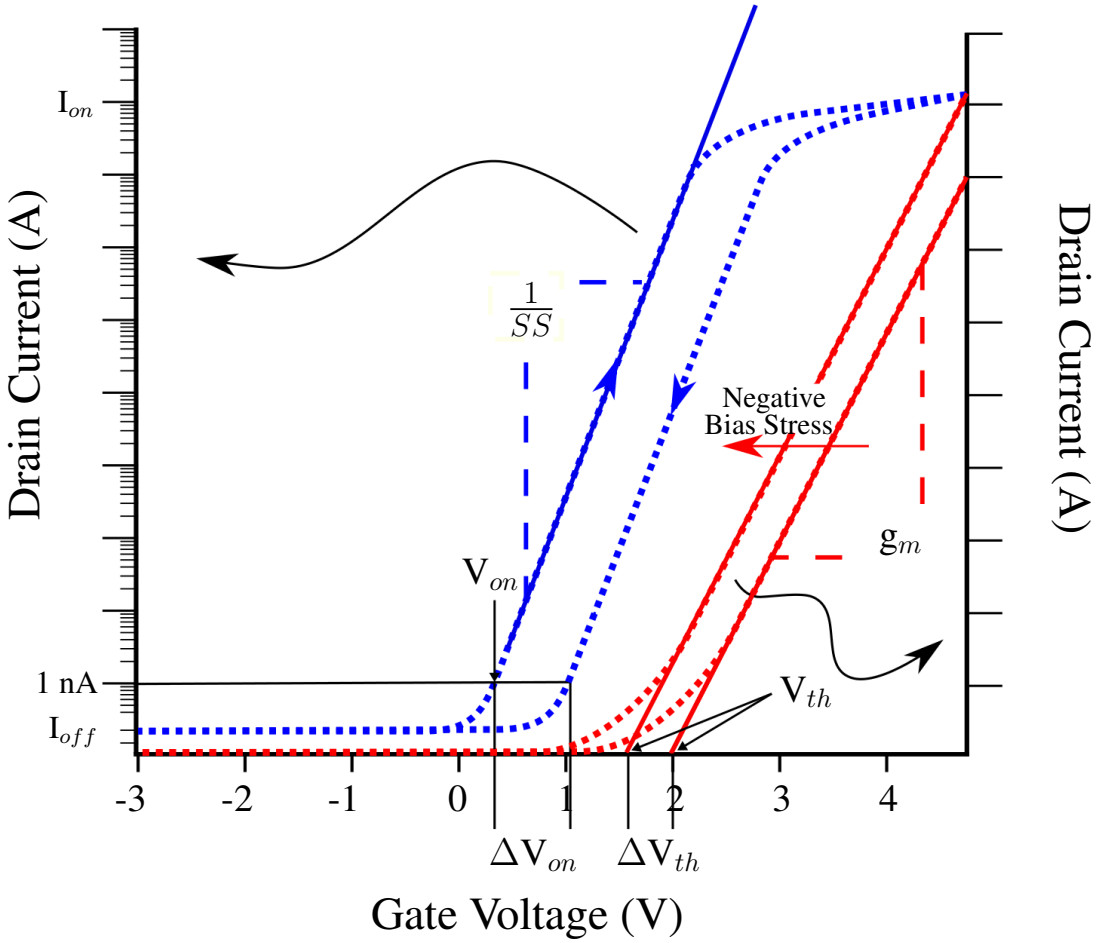


Figure 5.11: Schematic of an IV curve with KPI extraction points indicated, showing forward and reverse sweeps.

Turn-on and Threshold Voltage, V_{on} and V_{th}

The turn on voltage, V_{on}, is taken as the gate voltage applied when the drain current rises above 1 nA, while the threshold voltage, V_{th}, is taken as the gate voltage when the maximum tangent of the linear transfer curve is extrapolated back to intercept the x-axis, see figure 5.11. This is calculated by taking the gradient over each consecutive 10 points and choosing the greatest.

Mobility, μ

Mobility, μ, is the efficiency of carrier transport within a material, affected by scattering mechanisms such as impurities, grain boundaries, lattice vibrations, any many other structural deformities [33]. There are three different measures of mobility that can be applied: effective mobility, field effect mobility, and saturation mobility, each with advantages and disadvantages [26]. In this work, where mobility is discussed, this is measured as the field effect, μ_{FE}, calculated as

$$\mu_{FE} = \frac{g_m}{C_{ox}\frac{W}{L}V_D} \tag{5.4.21}$$

with L and W being the length and width of the channel, respectively, C_{ox} the gate dielectric capacitance, and g_m the conductance for low drain voltage, V_D taken as

$$g_m = \frac{\partial I_D}{\partial V_G}|_{V_D} \tag{5.4.22}$$

where V_G is the gate voltage and I_D is the current at the drain. In this work the transconductance, g_m, is taken as the maximum gradient of the linear transfer characteristic, found as above.

Sub-threshold Swing, SS

The sub-threshold swing, SS, is the inverse of the maximum slope of the logarithmic transfer curve, calculated as the maximum gradient of the logarithmic transfer characteristic again calculated by taking the gradient over each consecutive 10 points and choosing the greatest, see figure 5.11. SS is then

$$SS = \frac{1}{slope}. \tag{5.4.23}$$

Hysteresis

Hysteresis, the measure of the difference between the forward and reverse behaviour of the device, is calculated as the difference between V_{on} in the forward and reverse directions,

$$Hysteresis = V_{on_{forward}} - V_{on_{reverse}}. \tag{5.4.24}$$

Threshold Voltage Shift, ΔV_{th}

Threshold voltage shift, the measure of long term device stability, is similar to hysteresis but looking at V_{th} after prolonged application of a gate bias, so now

$$\Delta V_{th} = V_{th_{forward}} - V_{th_{reverse}} \tag{5.4.25}$$

Chapter 6

Optimisation of Aluminium Oxide deposited by Atomic Layer Deposition as Gate Dielectric Layer

In this chapter, a structural study of aluminium oxide layers for gate dielectric, deposited by atomic layer deposition (ALD), is presented. Control of gate dielectric deposition, and subsequent treatments, are of great importance as the quality of the dielectric layer is key to producing devices with good electrical characteristics and stability [26, 34, 141, 447, 448]

The gate dielectric is a thin layer of insulating material, with high dielectric constant, used to electrically isolate the conducting transistor gate electrode from the semiconducting layer. Two aspects of the gate dielectric are examined here, with work on optimisation of the ALD deposition parameters presented first, followed by consideration of the effects of thermal annealing on the deposited material.

Trilayer Aluminium Oxide deposited by Atomic Layer Deposition

The majority of the material structural analysis presented in this chapter is based on modelling of XRR measurements to obtain best-fitting representations of the film structure. It is therefore important to understand the intricacies of the XRR model. During initial work looking at ALD deposited aluminium oxide, it was found that the data were not well fitted by a simple model consisting of just a single layer of aluminium

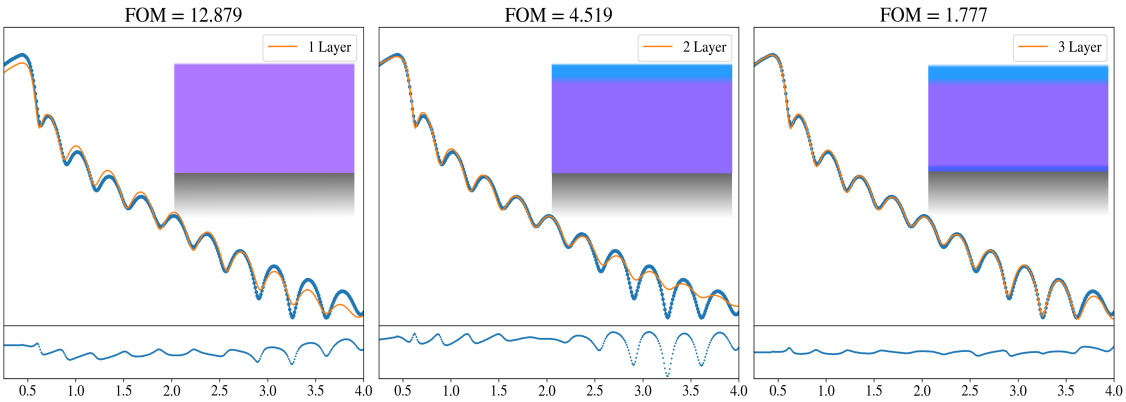


Figure 6.1: Fitting of 1, 2, and 3 layer models to the same XRR data for a 25 nm ALD aluminium oxide layer. Inset is a graphical depiction of the layer structures to scale, with variation in layer density represented by the colour. The fitting improves as more layers are introduced indicating the reducing figure of merit (FOM) value.

oxide on a silicon wafer (with or without an SiO_2 cap included in the model), see figure 6.1. Rather, it is shown that additional layers are required within the structural model to better represent the data. It was found that a two layer model improved the fitting but still lacked the precision required to get good results, so a range of layer numbers were tested. Figure 6.2 shows the calculated FOM value for the fitting of models with up to 10 layers. Here it can be seen that little improvement in the FOM is seen after the introduction of a third layer, and so this tri-layer structure was selected. This tri-layer structure also has good physical basis and can be understood as follows: at the interface between the deposited material and the substrate, the interaction between substrate and material dominates, with differences in kinetics and the presence of contaminants on the surface that combine to have an impact on the growth of the material. After sufficient material has been deposited, the influence of the substrate interface is diminished by the deposition of further material. In this region the highest quality, 'bulk', material is deposited. Finally, after deposition, the surface is exposed to environmental factors, where interactions with air can cause small changes in the surface material and environmental contaminants (such as organic matter) can quickly accumulate. This tri-layer model is supported by other published works, such as that from Hwang et al. who found a similar structure when looking at aluminium oxide deposited by ALD using synchrotron X-rays for their XRR [449]. Given the importance of understanding the material accurately, this tri-layer model was used for all fitting of the ALD aluminium oxide presented here.

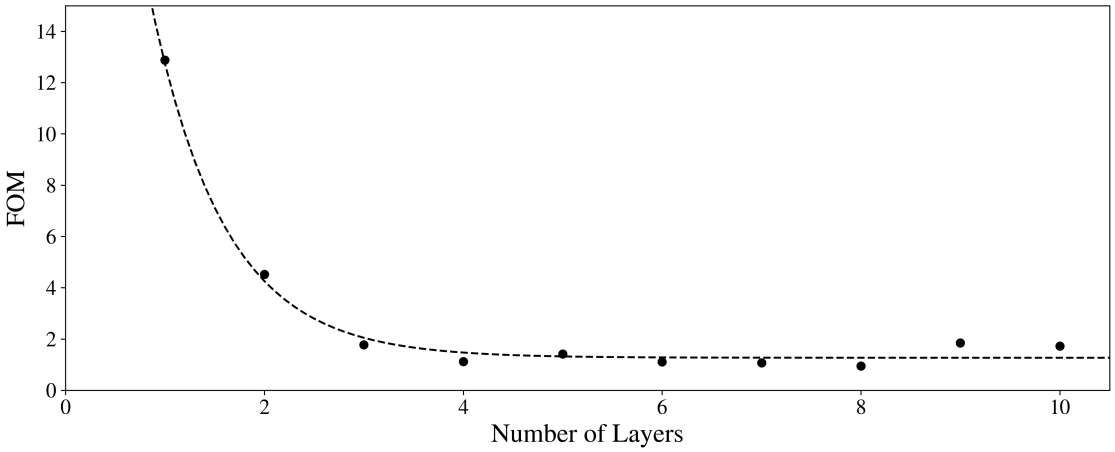


Figure 6.2: Figure of merit (FOM) values from fitting models with 1 to 10 layers to the XRR data presented in figure 6.1. The FOM quickly reduced as the number of layers is increased from 1 to 3, then plateaus as subsequent layers are added.

In order to compare samples in an easy to understand fashion, the total thickness of the three layers is quoted for the thickness, and the weighted average density is given for the layer density. These are calculated as

$$T_{total} = \sum_{i=1}^{3} T_{layer\ i} \tag{6.0.1}$$

and

$$\rho_{total} = \frac{\sum_{i=1}^{3}(T_{layer\ i} \times \rho_{layer\ i})}{T_{total}} \tag{6.0.2}$$

where T_i is the layer thickness and ρ_i that layer's density.

6.1 Optimisation of Atomic Layer Deposition Process Parameters for Aluminium Oxide

Chapter 4 presented an overview of the ALD technique and discussed the existence of optimal conditions for both temperature and pulse/purge times that should be established for the specific ALD facilities being used. In this section the optimisation of these processes is described and recommendations for the optimal conditions for the Beneq TFS500 system used here are presented.

6.1.1 Optimisation of the Precursor Pulse Time

The pulse times of the precursors are of great importance to the ALD process, particularly in a commercial setting. As discussed previously, pulse time is the time allowed to introduce the precursors. Times that are too short lead to incomplete layer deposition, while too long a time leads to wasted material and the potential for multilayered, rather than single atomic or molecular layer, deposition in each cycle. To investigate the optimal pulse times for both TMA and H_2O, for the multiwafer chamber in the Beneq TFS500 system, a series of depositions were performed with different pulse times while all other conditions were kept the same. This was done first for TMA, and then for H_2O. The "other" pulse time was set to the manufacturers recommended time and the gas purge times were set at values significantly longer than the expected optimum, to ensure they did not contribute to, or limit, the deposition process. Other variables were also kept at the standard settings as recommended by Beneq, such that the N_2 flow rate was 300 sccm for the precursor lines, and 400 sccm for the purge lines. The deposition temperature was set at 120 °C.

For each set of conditions two 1×1 cm pieces of single crystal (001) orientated silicon, with a thin native oxide coating, were placed in the reaction chamber at different heights. The deposition then consisted of 200 cycles of the ALD process. Each sample was subject to XRR measurements and the average materials values were determined, using the standard deviation over 4 measurements (each sample was measured twice) as the error on that value. The pulse and purge times for the investigation are shown in table 6.1.

While the discussion here is presented concurrently, it is worth noting that the optimisation of the TMA pulse time was done prior to that for the water pulse time. As such the pulse time of water during the TMA trial is held at 400 ms (the time recommended by the tool manufacturer). It was, however, found that the GPC in this trial was significantly lower that the expected 1 Å per cycle, likely due to the water pulse time being too short. As such, during optimisation of the water pulse, times longer than this where investigated while keeping the TMA pulse time well above the calculated optimum. The growth per cycle (GPC) and density of material deposited with varying

TMA and H_2O pulse times are shown in figure 6.3. Here the GPC is fitted with a function of the form

$$GPC = (1 - e^{-\lambda t}) \cdot GPC_{max} \tag{6.1.3}$$

where GPC_{max} is the maximum GPC reached, λ is a time constant for the increase in GPC, and t is time. This fit is used as it describes analytically the expected behaviour of the GPC here, i.e. a rapid increase in GPC as the volume of precursor entering the chamber nears the optimum level, followed by a plateau in the GPC when this optimum is reached. Knowing this expected behaviour, only a few samples are needed in order to extract the optimised values for precursor pulse times.

As the GPC follows an exponential curve the pulse time required to reach this maximum cannot be solved analytically, instead here we take the time required to reach GPC=GPC_{max}-α_{GPC}, where α_{GPC} is the 1σ confidence limit of the χ^2 fitted line, calculated using the methods presented in [435]. Using the values for GPC_{max}, the associated error, $\alpha_{GPC_{max}}$, and the value for λ, given in table 6.2, ideal pulse times (τ_{TMA}/τ_{H_2O}) can be calculated as

$$\tau = \frac{-1}{\lambda} ln \left(\frac{\alpha_{GPC_{max}}}{GPC_{max}} \right) \tag{6.1.4}$$

The results presented in figure 6.3 show the expected behaviour for GPC and density, in that the GPC follows equation 6.1.3 while the density remains constant, within error, for all samples. After fitting, values for GPC_{max} and λ were extracted and the optimum pulse times calculated using equation 6.1.4; these are presented in table 6.2. It should be

Table 6.1: Pulse and purge times for TMA and H_2O precursors during a study of the optimisation of the ALD pulse times of TMA (above) and H_2O (below)

TMA Pulse (ms)	TMA Purge (ms)	H_2O Pulse (ms)	H_2O Purge (ms)
100	7500	400	12500
400	7500	400	12500
600	7500	400	12500
800	7500	400	12500
TMA Pulse (ms)	**TMA Purge (ms)**	**H_2O Pulse (ms)**	**H_2O Purge (ms)**
700	7500	500	12500
700	7500	750	12500
700	7500	1000	12500

noted that the GPC_{max} found for the TMA pulse time was significantly lower than both the ideal GPC of 1 Å per cycle and the experimentally reported maximums of 0.9-1.1 Å per cycle [450–453]. This is may be due to a limiting H_2O pulse time; the pulse time of 400 ms, recommended by the tool manufacturer Beneq, was used for this trial, but this work shows that a significantly longer time, 1118 ms, was optimal for the H_2O pulse. This difference suggests that the H_2O pulse was likely reducing the GPC_{max} value during the TMA trial. It is worth noting too that, while the optimised pulse time for water is found to be greater that the times tested, this result is still valid as the suggested model, equation 6.1.3, fits well to the data.

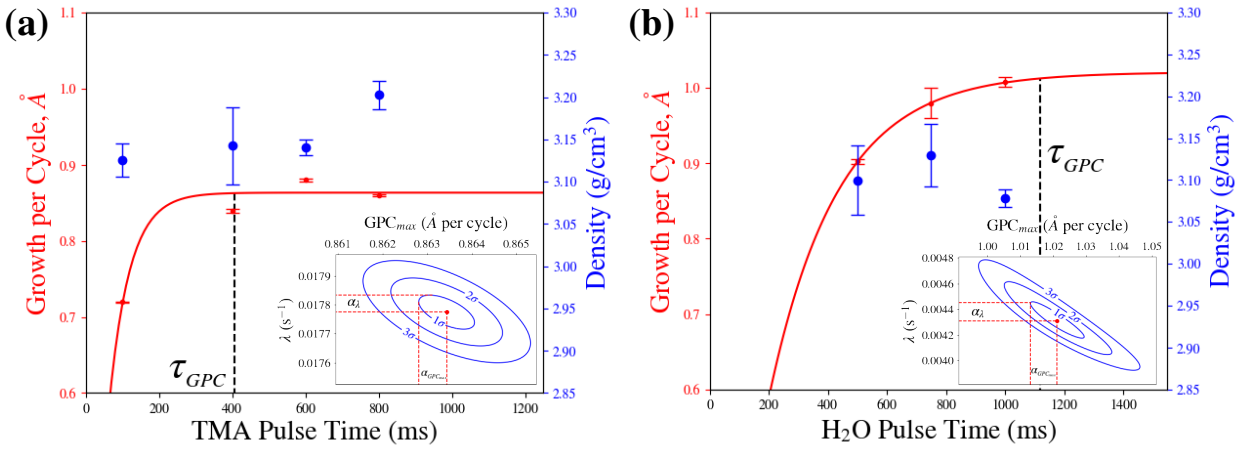


Figure 6.3: Growth per cycle and density of ALD deposited aluminium oxide films as a function of varying TMA **(a)** and H_2O **(b)** pulse times with all other parameters fixed. The solid line shows χ^2 minimised fits for the GPC using equations 6.1.3. Inset contour plots of the 1σ, 2σ, and 3σ uncertainty levels from the χ^2 fitting, with the 1σ limits presented in table 6.2.

Table 6.2: Results of χ^2 best fitting of equation 6.1.4 with associated errors for GPC with precursor pulse time variation.

Parameter	**TMA**		**H_2O**	
GPC_{max} (Å/cycle)	0.8634	±0.0006	1.021	±0.008
λ (ms^{-1})	0.01777	±0.00006	0.0043	±0.0001
τ (ms)	407		1118	

6.1.2 Optimisation of the Purge Gas Times

Following optimisation of precursor pulse times, the purge times for each cycle was optimised. This was done both to minimise processing time and to reduce the possibility of precursor desorption during purging. A similar methodology was followed to that used for pulse time optimisation. However, when considering purge times, the GPC and density are expected to follow different trends. Now it is expected that with very short purge times a thick layer of low quality material will be deposited, since residual precursor and by-product may be present. This in turn means the film may have lower density. As the purge time is increased, more contaminants are removed and a thinner, higher quality (and therefore higher density) film results. In this case the GPC is expected to follow a trend of the form

$$GPC = \left(GPC_{extra} \times e^{-\lambda t}\right) + GPC_{opt} \tag{6.1.5}$$

where GPC_{extra} is the additional material deposited in each cycle due to the inclusion of impurities, GPC_{opt} is the optimal growth per cycle at very long purge times, and λ is again the characteristic time to reach optimal conditions. This again provides an analytic description of the expected behaviour, meaning the number of samples required can be keep low. As the density now increases to an optimal value, this can be described similarly with

$$\rho = (1 - e^{-\lambda t})\rho_{max} \tag{6.1.6}$$

where λ is again a characteristic time, and ρ_{max} is the maximum density. Following the same reasoning that lead to equation 6.1.4, equations can be found for the purge times using either the GPC,

$$\tau = \frac{-1}{\lambda} ln \left(\frac{\alpha_{GPC_{opt}}}{GPC_{extra}} \right) \tag{6.1.7}$$

or the density

$$\tau = \frac{-1}{\lambda} ln \left(\frac{\alpha_{\rho_{max}}}{\rho_{max}} \right) \tag{6.1.8}$$

where α denotes the error in the value, found using the same methodology as was used previously. The pulse and purge times used are shown in table 6.3. The resulting density and thickness obtained from best fitting simulations to the XRR data are shown in figure 6.4, and the extracted values and their uncertainties given in tables 6.4 and 6.5.

Table 6.3: Pulse and purge times for TMA and H_2O during optimisation of purge times following TMA (above) and H_2O (below) pulses.

TMA Pulse (ms)	TMA Purge (ms)	H_2O Pulse (ms)	H_2O Purge (ms)
700	2500	1000	20000
700	5000	1000	20000
700	7500	1000	20000
700	10000	1000	20000
TMA Pulse (ms)	**TMA Purge (ms)**	**H_2O Pulse (ms)**	**H_2O Purge (ms)**
700	10000	1000	5000
700	10000	1000	7500
700	10000	1000	10000
700	10000	1000	12500
700	10000	1000	15000

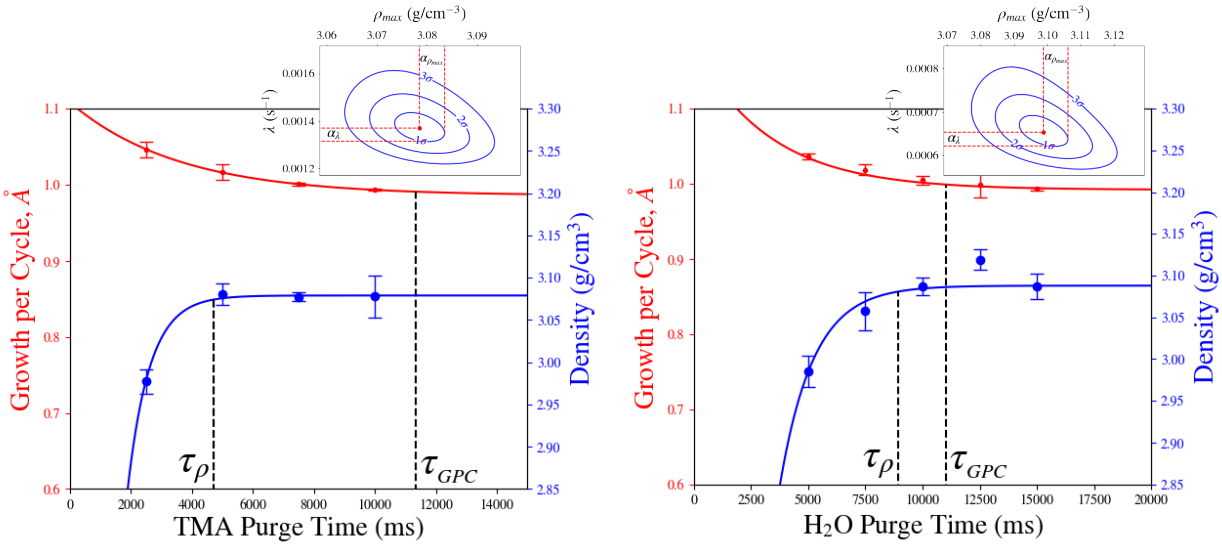


Figure 6.4: Growth per cycles and density of deposited films with varying purge times after TMA (left) and H_2O (right) pulses. The solid line shows χ^2 minimised fits for the GPC and density using equations 6.1.7 and 6.1.8 respectively. Dotted lines indicate the optimal purge times, τ, from the GPC and density fitting. Inset contour plots of the 1σ, 2σ, and 3σ certainty levels for the χ^2 fitting for the density, with the extraction of the 1σ limits, presented in table 6.5 shown.

It is worth noting from these results, the difference in the optimal purge times, τ. The values for τ calculated from fitting equations 6.1.7 and 6.1.8 show significant difference, as seen in figure 6.4. This difference requires careful consideration of the origin of density and GPC changes. As discussed previously, during purging there is a possibility that precursors may desorb from the surface, and the likelihood of this increases with purge time, thereby reducing the GPC for long purge times. Conversely, the density of the

Table 6.4: Results of fitting data to equation 6.1.7 with associated errors for GPC with purge time.

Parameter	TMA		H_2O	
GPC_{extra} (Å/cycle)	0.12	±0.03	0.190	±0.05
λ (ms^{-1})	0.0003	±0.0001	0.0003	± 0.0001
GPC_{opt} (Å/cycle)	0.986	±0.005	0.992	±0.008
τ (ms)	11355		11043	

Table 6.5: Results of fitting data to equation 6.1.8 with associated errors for density with purge time.

Parameter	TMA		H_2O	
ρ_{max} (g/cm^-3)	3.079	±0.005	3.088	±0.007
λ (ms^{-1})	0.00137	± 0.00006	0.00068	± 0.00004
τ (ms)	4700		8950	

material deposited will not be affected by any desorption of precursors, meaning longer purge times will not cause a variation in density after the point at which pure single layer deposition occurs. This suggests that some desorption of precursors occurs during the purge here, which leads to a difference in the values of τ calculated from the GPC and density data. This is additionally evidenced by the fact that the GPC in the long purge regime (here called GPC_{opt}), is lower than the ideal ALD growth rate of 1 Å per cycle, indicating the deposition of incomplete layers. This difference is most pronounced in the TMA purge times, where there is a difference of 6655 ms, due to the higher volatility of TMA compared to H_2O.

In addition to the above discussion the difference in the confidence levels found through fitting for the density and GPC should be considered. While the error calculated for GPC_{opt} and ρ_{opt} are similar (around 0.5%), the error on λ is significantly higher in the fitting for GPC at around 33% compared to around 5% for the fitting with density.

In the context of transistor device production in this work, where the ALD aluminium oxide is used as the gate dielectric, the quality of the ALD layer is paramount, and a strong understanding of the optimised conditions essential. As such, the density of the film should take precedence and so the purge times calculated from the density should be used.

The work presented in this section should be viewed as a complete methodology for the

optimisation of pulse and purge times for an ALD system, and should be repeated in some form when any variations in the ALD process are introduced, such as changes in hardware, temperature, or the precursors.

6.1.3 Optimisation of Substrate Temperature during Atomic Layer Deposition of Aluminium Oxide

Having established optimal pulse and purge times for the ALD process, the other necessary optimisation step is for processing temperature. As discussed in section 4.1.2.1, there are several possible regimes in which the atomic deposition process can operate, dependent on temperature. In order to establish the optimal conditions, a trial was run to look at ALD aluminium oxide deposited at different process temperatures. For this, samples of single crystal (001) orientated silicon wafer, with a thin native oxide layer, were placed in the reaction chamber of a Beneq TFS200 ALD tool at Cambridge University. The processing was carried out by engineers from Pragmatic. It should be noted that, while the pulse and purge times needed for this work were different due to the change away from the normal TFS500 system, the effect of temperature is expected to be the same.

For this, 410 cycles of the ALD process were performed with the following pulse/purge times:

- TMA pulse time: 250 ms
- N_2 TMA purge time: 2500 ms
- H_2O pulse time: 400 ms
- N_2 H_2O purge time: 2500 ms

The reaction chamber temperatures used were 150 °C, 200 °C, and 250 °C. The conditions for each temperature were repeated three times to establish any variability between the depositions. Figure 6.5 shows the measured data for both the GPC and film density. From this it can be seen that the GPC reaches a maximum at 200 °C, while the density appears to plateau above this temperature. This behaviour is consistent with the process window lying around 200 °C. Temperatures below this produce incomplete and low quality layers

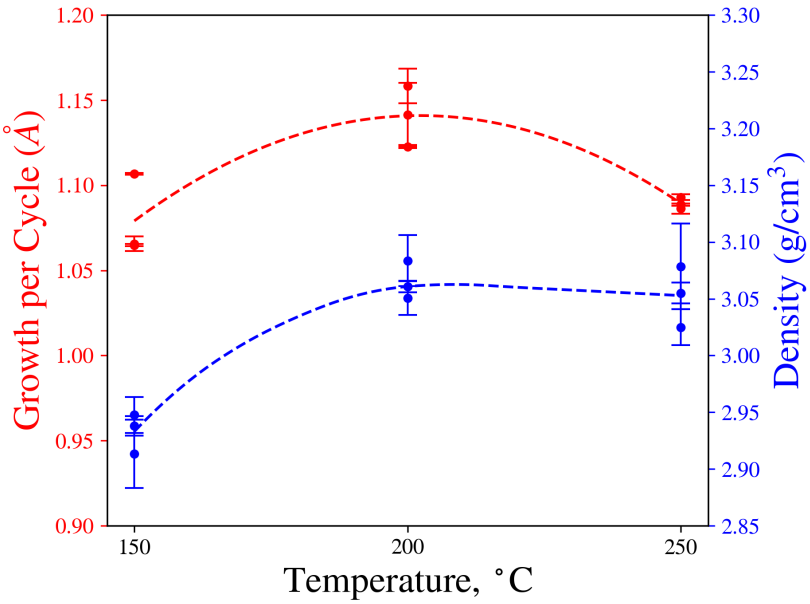


Figure 6.5: GPC and film density with varying ALD temperatures for aluminium oxide. Three runs are shown for each temperature with the error bars representing the variation in XRR fitted data over multiple repeated measurements of each sample. Dotted lines are included as guide to the eye.

and therefore reduced GPC and density, while temperatures above this lead to desorption of the precursors preventing full coverage on every cycle without degrading the quality of the film. From this it can be concluded that 200 °C should be used as the ALD processing temperature for deposition of aluminium oxide gate dielectric.

6.2 Post Deposition Annealing of Aluminium Oxide deposited by Atomic Layer Deposition

Many published studies [452, 454, 455] have shown that the quality of amorphous aluminium oxide can be improved though thermal annealing in a variety of ambient conditions. These improvements take the form of reduced surface roughness, reduced pin-holing, increased density, or a combination of all of these.

To see if thermal annealing can have any such effect on the ALD material studied here, while remaining within the temperature range acceptable for the processing of flexible substrates, a trial was run. Here samples of $\sim$ 45 nm ALD aluminium oxide where deposited under optimised conditions in the Beneq TFS500 tool, on single crystal silicon

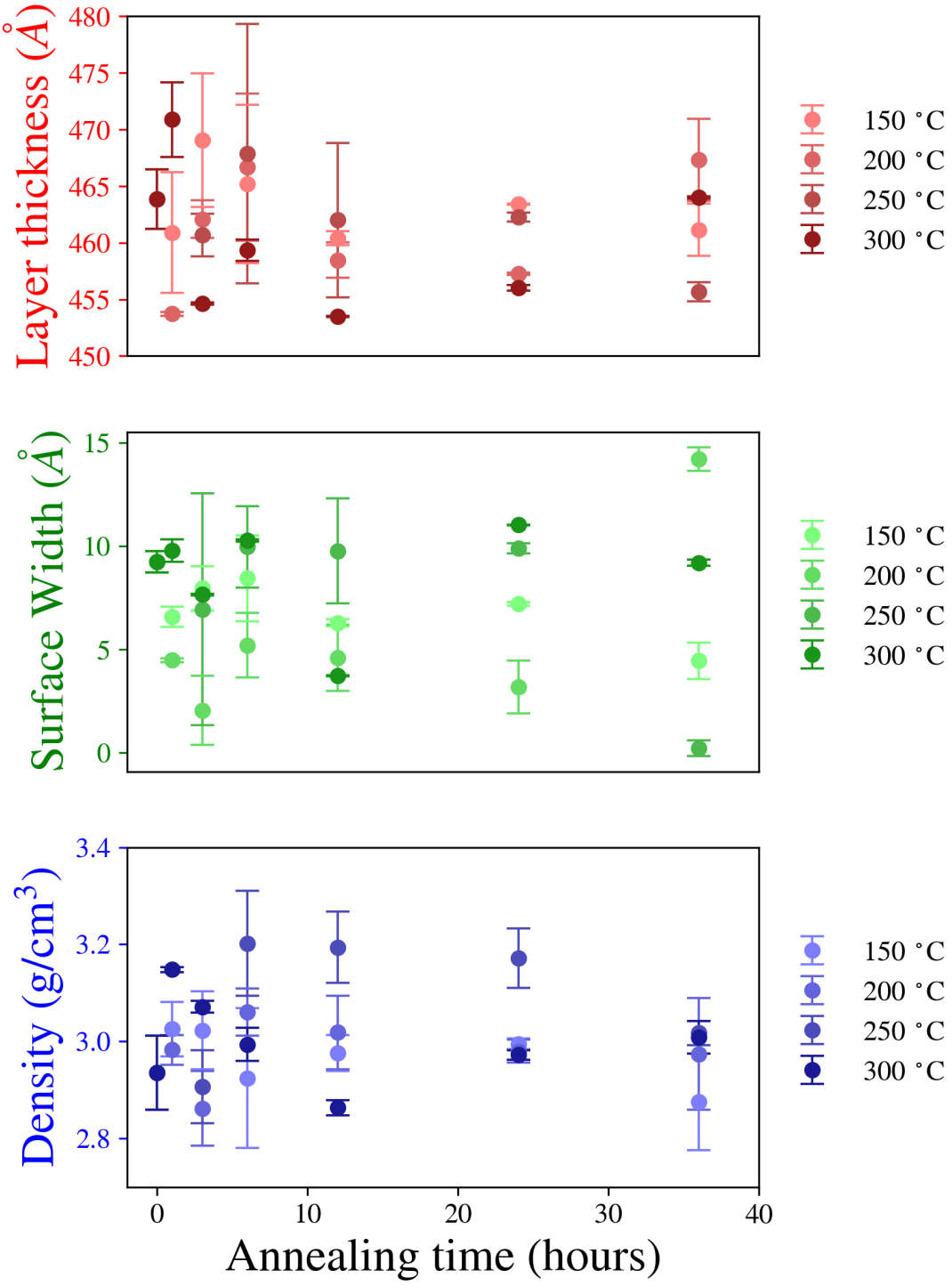


Figure 6.6: Thickness (red), density (blue), and surface width (green) for ALD deposited aluminium oxide annealed in air between 150 °C and 300 °C.

wafer pieces, using 420 ALD cycles with the batch processing chamber. These samples were annealed between 150 °C and 300 °C for up to 36 hours. This annealing was carried out in air at atmospheric pressure using a Carbolite HTCR5/28 oven. Figure 6.6 shows the thickness, density and top surface width for the material, obtained from XRR fitting after annealing. It can be seen that there is very little variation in any of these parameters with annealing as a function of time, indicating that a post deposition annealing step does not improve the properties and is therefore not required in the production process.

6.3 Conclusions

In this chapter, a systematic study of the deposition and annealing of aluminium oxide by atomic layer deposition, for use as a gate dielectric, was presented. The first section presents methods for optimising the deposition cycle times and temperatures in order to achieve optimal growth conditions compatible with flexible substrates. This included the recommended procedures for obtaining the necessary data, a thorough discussion of the analysis of such data, and extraction of optimal parameters. As well as presenting methods to be used in the future, the work suggests ideal parameters for the systems discussed.
This methodology for optimisation should be applied whenever a significant alteration to the experimental set-up is made, including changes to the reaction chamber, operating temperature, or precursor supply. In addition, post deposition annealing, compatible with flexible substrates, was investigated and found to have little observable effect on the material.

Chapter 7

Comparative study of Aluminium Oxide deposited by Sputtering and Atomic Layer Deposition for use as an insulating buffer

As discussed in section 3.3.2.3, in the top contact, coplanar device configuration used in this work it is common to include a layer of an insulating buffer material which the semiconducting layer sits on top of, used to prevent permeation of water and gases from the flexible substrate [209, 210, 212]. While in principle this layer should not show any electrical behaviour itself, it can significantly affect the performance of devices through interaction with the back side of the channel material [189, 213, 271, 456, 457]. This is similar to the more widely studied back-channel effects seen in bottom gate transistor architectures, except that the penetration of ambient gases at the interface is greatly reduced since the back-channel here never sees ambient conditions [15, 249, 458–460]. In this work aluminium oxide was used to form this buffer layer with low surface roughness and good electrical insulting properties, onto which IGZO semiconductor was deposited. In current fabrication processes this layer is deposited through physical vapour deposition (PVD) methods. However, looking forward, to reduce the number of tools required for device fabrication, and to allow for introduction of complementary semiconductors (a p-type semiconductor which can be used in conjunction with the n-type IGZO to

create a CMOS architecture), there are drives to develop an aluminium oxide buffer layer deposited by atomic layer deposition (ALD). To date this has not been viable due to degradation of device performance when an ALD buffer is used rather than PVD material. Such devices are highly conductive and do not show switching behaviour within the limits of testing. The following work is a comparative study that attempts to understand the difference between the materials deposited by PVD and ALD in terms of their structural properties in relation to device performance. In order to study this samples made by reactive sputtering from an aluminium target withan oxygen atmosphere are compared to samples produced with the same ALD process as that discussed in chapter 6.

7.0.1 Multilayer Model for X-ray Reflectivity fitting of Sputtered Aluminium Oxide

Figure 7.1 shows an X-ray reflectivity (XRR) scan typical of the sputtered aluminium oxide studied here. On examination of the data it can be seen that, in addition to the normal Keissig fringes, a further enhancement of the data exists at around 2.9°. This enhancement is interpreted as a Bragg peak, which indicates that the film has a superlattice structure indicative of the interference from multiple repeated layers that constitute the film. To examine this, models of one layer, three layers, and multiple layers (where the number of layers is allowed to vary as a free parameter) are presented in figure 7.1. From this analysis it is clear that the multilayer structure fits the data far better than single or tri-layer structures. Additionally, it was found that optimal fitting was achieved at around 20 layers. As discussed in chapter 4, the sputter deposition process involves cyclic sweeping of the substrate in front of the target during deposition, which here consists of 20 sweeps. This means the wafer pallet is moved across the sputtering target 20 times, at 120 cm per minute. As the number of layers in the fit matches the number of scans during deposition, can be concluded that the multiple sub-layers each correspond to a single deposition pass. Here, each sub-layer comprises a “thick” region of normal density material, atop a “thin” region of lower density material. It is suggested that this low density layer occurs due to contamination from material, such as moisture and organic contaminants, within the sputtering system, when the sample is at the extremity of its travel during deposition. While the variation in X-ray scattering length density (SLD)

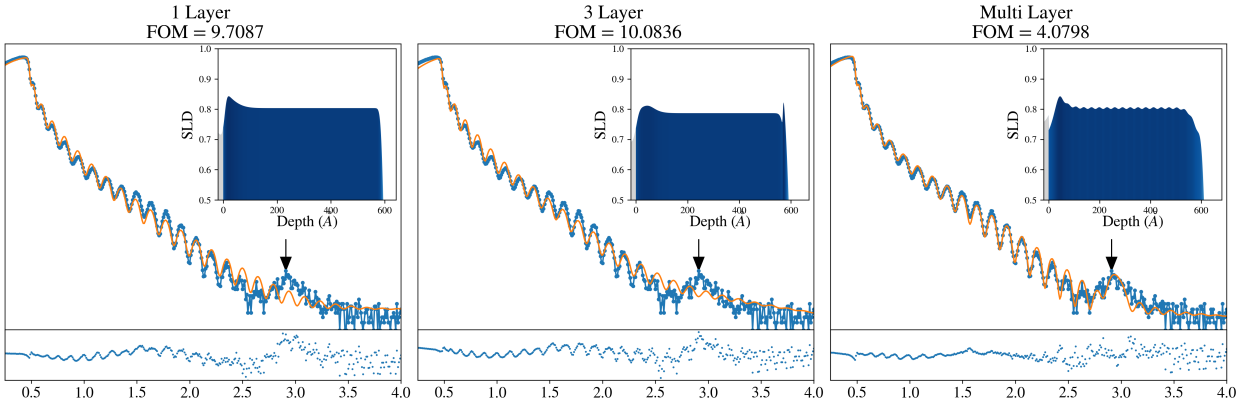


Figure 7.1: XRR fits for sputter deposited aluminium oxide, using 1 layer, 3 layer, and multilayer models. Inset is the scattering length density (SLD) profile, a measure of the material density, with variations in SLD shown through both the height on the y axis and the colour of the fill, with 0 Å depth being the substrate interface. Below each XRR plot is shown the residuals for the plots, with the multilayer model showing the least structure, corresponding to the lowest FOM, and therefore the best fit. Arrow at ~2.9° indicates the Bragg peak.

across a sub-layer is small, due to the large "width", or diffuse nature, of the interface between thick (~30 Å) high density and thin (<1 Å) low density regions, it is significant enough for XRR detection. This variation can, therefore, be used as a comparative measure between samples.

As with the tri-layer structure of the ALD material discussed in chapter 6, when sample thicknesses and densities are discussed here, these represent the total thickness of all the sub-layers combined and the weighted average density across the whole film respectively, calculated as

$$T_{total} = \sum_{i=1}^{n} T_{layer\ i} \tag{7.0.1}$$

and

$$\rho_{total} = \frac{\sum_{i=1}^{n}(T_{layer\ i} \times \rho_{layer\ i})}{T_{total}}. \tag{7.0.2}$$

where n is the number of sub-layers.

7.0.2 Variation in Sputtered Material Proprieties with Time of Deposition in working week

Examination of historical production data has shown some variation in the performance for devices produced on buffer material deposited on different days of the week. In order

to understand this and explore any connection to physical differences in the sputtered buffer, and to establish if this in turn corresponds to the degraded behaviour seen with ALD material, samples of sputtered material were examined from the beginning and end of the production facility's working week, i.e. a Monday and a Friday. For this comparison, samples of the standard (001) orientated silicon material were included in the buffer sputtering run for device production. Samples were placed in gaps on the pallet between circular wafers to ensure the the samples were representative of the material in the devices. Data suggests that devices fabricated with material deposited on a Friday (after 5 days of tool use) showed degraded performance compared to devices fabricated on material deposited on a Monday (after a 2 day break in tool use over the weekend). To examine this samples were taken from a Friday and the following Monday (exactly 72 hours later). The sputtering parameters were the same for both depositions with the exception of the chamber base pressure which was 0.213 mPa for the Friday deposition and 0.096 mPa for the Monday deposition.

Material from Friday vs Monday

Examples of the measured XRR data, the best fitting simulations, and the resulting SLD profiles for the samples taken from Friday and Monday are shown in figure 7.2 and the best fitting parameters are given in table 7.1. From inspection of the XRR data it can be seen that the Bragg peak is more pronounced in the Friday sample. This is reflected in the more obvious sub-layers in the SLD profile for the sample, and the order of magnitude difference in density variation (the difference between the high and low density regions within the sub-layers). In addition the overall density of the Monday sample is higher and the thickness lower, suggesting a more stoichiometric film with fewer impurities and defects. The differences observed may be explained by differences in the chamber base pressure on Friday compared to Monday. The base pressure of 0.213 mPa on Friday is more than twice that on Monday (0.096 mPa), meaning there is a higher level of contaminants within the system that are likely to cause difference in the film quality. This is particularly significant in the low density regions of the sub-layers, where more contaminants may be included in the film at the extremities of the wafer pallets' travel where the deposition rate is lower. The difference in base pressure is most likely due to

the extended evacuation period over the weekend. This clearly demonstrates the need for tighter control of the chamber base pressure, perhaps lowering the maximum acceptable base pressure to that present on Mondays. This is further exemplified when differences in measured device performance are considered. For example 45 identical devices on wafers from each day where measured, these devices where in the same position on the wafer and had all other process steps performed in tandem. Of these devices 3 were excluded from the Friday wafer and 5 from the Monday wafer due to device failures (no switching behaviour seen at all). Figure 7.2 shows median IV curves for device, while curves for all devices are not shown due to commercial sensitivity, those shown indicative of the general behaviour of all the devices in each batch. Of the devices, those from the Friday wafer showed significantly higher sub-threshold swing, SS, with the devices on material from Monday having an average value of just 51% of the average from Friday. The average mobility for the Friday devices is also 31% lower, while the hysteresis seen in these devices is 5.5 times that seen in the Monday devices. These devices received identical treatment with the exception of the buffer deposition date, demonstrating the importance of this buffer layer.

7.1 Comparative study of Atomic Layer Deposition and Sputter Deposition of Aluminium Oxide for device Buffer layers

The above discussion helps with an understanding of the buffer material. However, as discussed previously, there is a drive to replace this PVD material with ALD material.

Table 7.1: Results from GenX fitting of XRR data for aluminium oxide samples deposited on a Friday and the following Monday. Density Variation here is the difference in density between the low and high density regions of the sub-layers.

	Monday	**Friday**
Surface Roughness (Å)	10.7±0.2	14.2±0.5
Thickness (Å)	566±1	633±2
Density (g/cm^3)	2.83±0.02	2.69±0.03
Density Variation (g/cm^3)	0.06±0.02	0.67±0.04

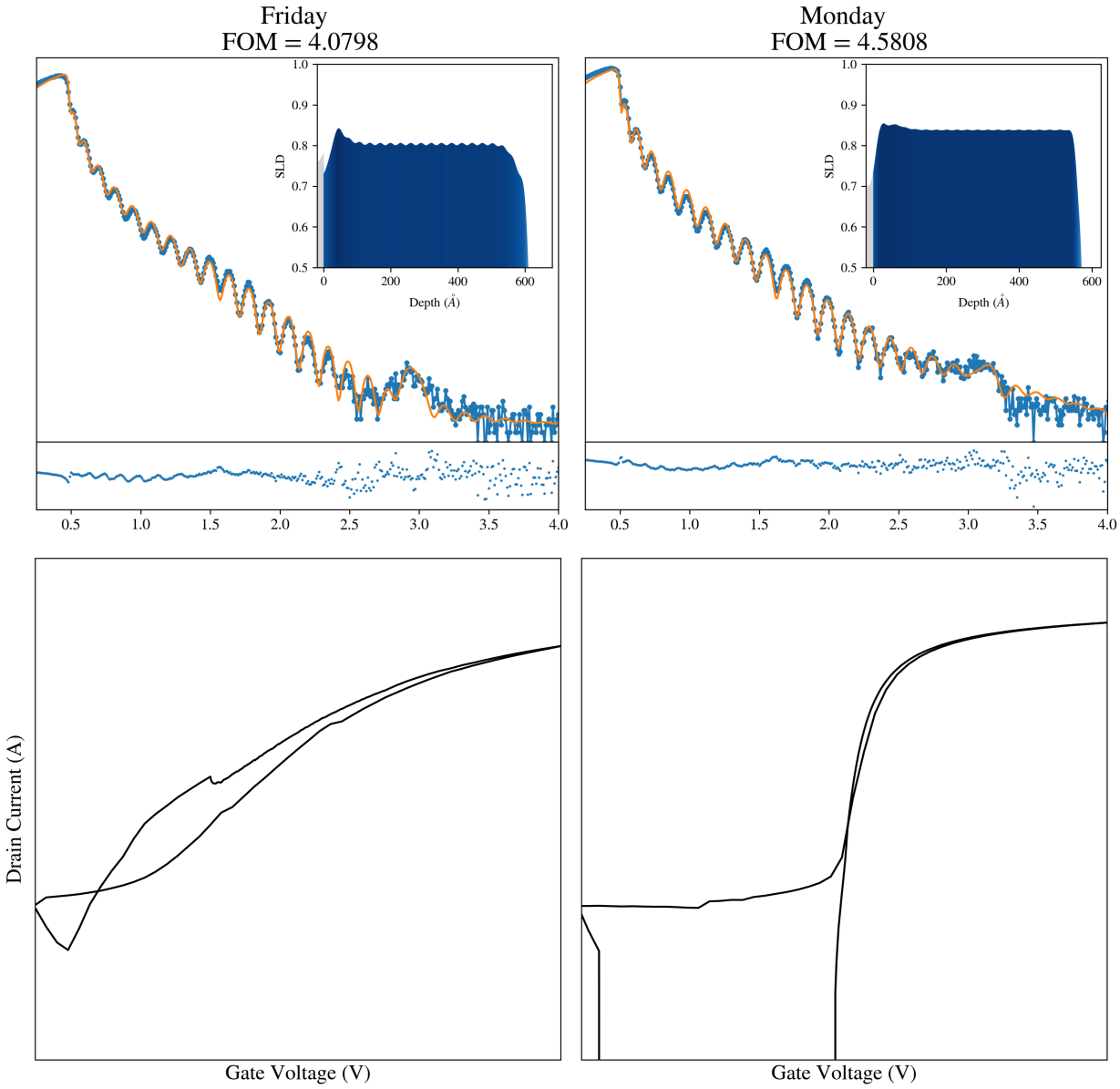


Figure 7.2: XRR fits for sputter deposited aluminium oxide deposited on a Friday and a Monday. Inset is the scattering length density (SLD) profile, a measure of the material density, with variations in SLD shown through both the height on the y axis and the colour of the fill, with 0 Å depth being the substrate interface. Below each XRR plot are shown the residuals for the plots. Below each XRR are representative transfer curves for 10×1 μm (W×L) devices produced on wafers with buffer deposited during the Friday and Monday runs examined above.

To date the ALD material has been unsuitable for this application. The following work looks at different comparisons between sputtered and ALD aluminium oxide in an attempt to understand the origins of the different functional performance with ALD and PVD aluminium oxide buffer layers.

7.1.1 Direct comparison of buffer material deposited by Atomic Layer Deposition and Sputtering

The starting point for comparison between sputter and ALD deposited material is the parameters probed through XRR - density, thickness, and interface widths. Of these, it is particularly the material density and the surface structuring that are considered most likely to have an effect on device performance, due to the introduction of trapping sites at the interface. Initially, comparisons are made between as-deposited materials and material that has received the same processing as used in device fabrication. For comparison, here samples of ALD and sputtered aluminium oxide with a target thickness of 50 nm are compared. Results of the best fitting XRR models are given in table 7.2. The results of XRR comparison of the as-deposited materials, in table 7.2, show a somewhat counter intuitive picture with regards to the difference in device performance. The ALD aluminium oxide material has a higher overall density, and smoother surface, than the sputter deposited material. While these measurements are consistent with results presented elsewhere in literature [212, 461–463], they do not match what is expected based on device behaviour. From previously reported finding it was expected that devices which showed the best electrical characteristics would have been those deposited on high density, smooth material [198, 213, 464]. This is attributed to there being fewer trap sites in the layer and at the interface. However, here we find that the better devices are those produced on the lower density and rougher sputter deposited material. This,

Table 7.2: Results extracted from XRR fitting for ALD and sputter deposited aluminium oxide.

	ALD	**Sputtered**
Thickness from XRR (nm)	52.4± 0.2	60.8±0.4
Density (g/cm^3)	3.12 ±0.04	2.86 ±0.03
Top Interface from XRR (nm)	0.5±0.1	2.1±0.1

therefore suggests that either the physical characteristics of the buffer layer do not affect the electrical properties of devices, or that the devices benefit in some regard from these imperfections. Further investigation of the difference between the materials is therefore required in future work.

7.2 Surface Energy

During sputter deposition of IGZO, one factor that affects the structure of the newly created interface is the energetics of the adsorbed material. These energetics are governed by both the energy of the material, and its interaction with the surface to which it has adsorbed. This in turn means the surface energy of the deposited material has an influence on the structure of the interface.

In order to investigate the difference in device performance for sputtered and ALD buffers, this surface energy was investigated using contact angle measurements, as described in section 5.3. As the energetic interaction of a material with a surface can be highly sensitive to any treatment that the surface receives, conditions representative of standard processing steps were employed in order to understand the behaviour of these materials. This included, in addition to investigating the 'as-deposited' material, samples that were annealed at 300 °C for 1 hour in ambient atmosphere, and samples that received this anneal followed by deposition and removal of an additional metal oxide layer by sputtering and etching in oxalic acid for 210 s.

For this, one silicon wafer was coated with ALD aluminium oxide, and a second with sputtered aluminium oxide, using the standard conditions for these depositions discussed previously. These were subsequently cleaved, with one piece from each wafer receiving no further treatment, one piece receiving the anneal step, and a third piece receiving the anneal step followed by the sputter deposition of an additional layer which was then removed by etching in oxalic acid, as summarised in tables of figure 7.3.

Figure 7.3 shows contact angle results for each sample with the regression lines as discussed in chapter 5.3, with the calculated surface energy components given in tables inset. Here it can be seen that the total surface energy for the two deposition methods is similar for all treatments, and that each treatment has a somewhat similar effect on

the two types of material. The values of surface energy and its components, particularly for the unannealed material, are in good agreement with previously published data from similar measurements [465, 466].

However, it is interesting to note the size of the effect of each treatment on the two components of surface energy. For ALD material, annealing alone has a significant effect on the dispersive component of the surface energy, but little effect on the polar component. Subsequent layer deposition and etching then has just a small effect on the dispersive component, but causes a more pronounced increase in the polar component. Conversely, for sputter deposited material annealing causes a significant reduction in the dispersive component and a marked increase in the polar component. Subsequent deposition and etching then increases the dispersive component again, as well as further increasing the polar component.

As the dispersive and polar components of the surface energy refer to interactions between temporary dipole moments (London dispersion forces [467–469]) and fixed dipole moments respectively [470], these differences in behaviour allow for some speculation as to physical processes occurring and their impacts on devices. For ALD material, annealing increases the dispersive component, indicating the presence of less tightly bound electrons at the surface. This may be due to the effusion of non-polar impurities, such as hydrogen, trapped during deposition [52, 461]. As these move to the surface they may provide more sites where temporary dipoles can be induced, contributing to the dispersive components. This is hinted at by previously conducted thermal desorption spectroscopy (TDS) of ALD deposited aluminium oxide (data not shown) and could be further tested by annealing the material at different temperatures and repeating these contact angle measurements. The etching process, on the other hand, has little impact on the dispersive component for ALD material, but does have a large effect on the polar component. As this polar component is due to the presence of fixed dipoles, this indicates an increased density of such charges at the surface. A likely reason for this is that either the deposition sputtering of the additional layer, or its subsequent removal by etching, breaks some of the metal-oxygen bonds at the sample surface leaving dangling bonds with fixed charges that substantially increase the polar component of the surface energy.

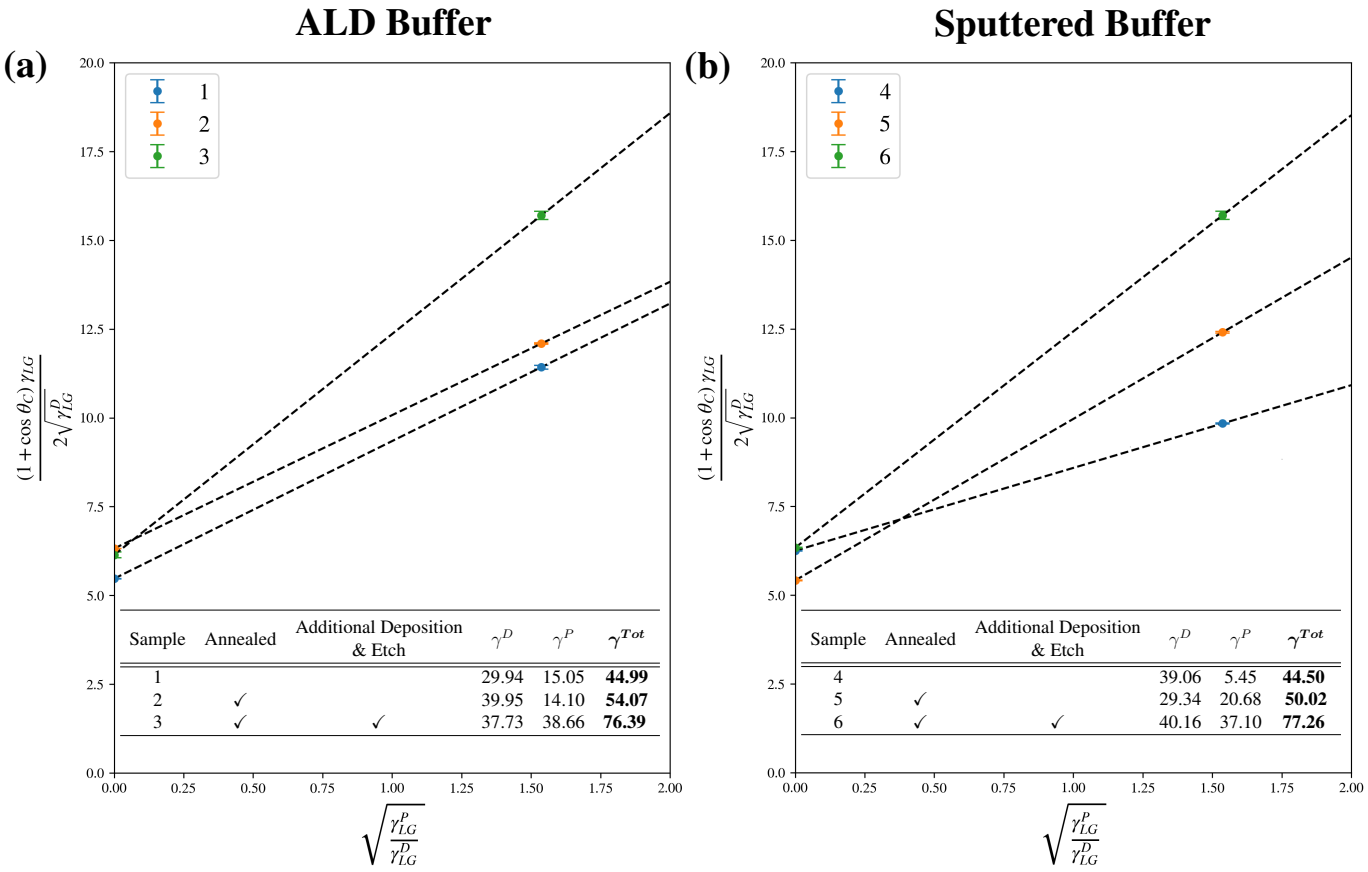


Figure 7.3: Regression plots for the surface energy of **(a)** ALD and **(b)** sputtered aluminium oxide with various treatments. Inset tables give the post deposition treatment of each sample along with the polar and dispersive components, along with the total surface energy, for each sample in mN/m.

While the as-deposited and fully processed sputtered samples have similar total surface energies to those seen in ALD material, how these are reached differs markedly. The initial dispersive and polar components are significantly different, suggesting a lower concentration of permanent dipoles, but a higher presence of dispersive sites. This may be due to the inclusion of excess oxygen in the sputter deposited material compared to ALD, which may result from reactive sputtering processes and should be investigated through the use of XPS and TDS. The annealing step here reduces the dispersive component and increases the polar component, supporting the supposition that excess oxygen was initially incorporated, but is released during the annealing step. Finally, the deposition of an additional layer and subsequent etching process increases both the dispersive and polar components. As with the ALD material, it is likely that the increase in the polar component is due to the breaking of metal-oxygen bonds during either the

metal oxide deposition or its subsequent removal. The reason for the increase in the dispersive component, to just above its original level, is less clear but may be due to adsorption of water or other surface contaminants during the etching process.

While this work does not provide a clear explanation for the difference in behaviour of devices fabricated on sputter and ALD deposited material, as the surface energy for each and their components are similar, particularly for the material treated analogously to that which is used in devices, it does provide some interesting insight into the behaviour of the materials during the preparation process.

7.3 Conclusions

In this chapter deposition of aluminium oxide as a buffer material has been discussed. While the buffer material should notionally have little effect on device performance, it is seen that device performance is in fact highly sensitive to the method of deposition used. Attempts were made to find the origin of this sensitivity, looking at physical differences between ALD and sputter deposited materials. The material structure was studied, through XRR, finding markedly different structures within the layer itself, but little difference at the surface in contact with the semiconductor. The chapter also looks at differences between sputtered material deposited in systems with different base pressures, corresponding to different times of the week, and found devices fabricated on material deposited with a higher base pressure showed more pronounced layer sub-layer and degraded device performance. Finally, comparisons were made between surface energies for ALD and sputtered aluminium oxide, showing some difference in energy components for untreated devices, but surprising similarity between materials when prepared as for device fabrication.

This work does not identify a single clear reason that can explain the the difference in device performance through the methods used here, suggesting some more in-depth exploration is required to elucidate the reason for this difference. These techniques may include thermal desorption spectroscopy (TDS) to examine trapped gaseous species and impurities, Secondary Ion Mass Spectroscopy (SIMS) or X-ray Photoelectron Spectroscopy (XPS) to examine layer stoichiometry and atomic bonding environments,

and Scanning Tunnelling Microscopy (STM) to probe local electrostatic environments. Moving forward, examination of this surface when in contact with the semiconducting layer is needed as this may provide routes to remove the difference in performance. This is examined in chapter 9.

Chapter 8

Densification of sputtered amorphous In-Ga-Zn-O through thermal annealing compatible with flexible substrates

The electrical properties of the semiconducting layer in a transistor are key to the device characteristics. These electrical properties are, in turn, governed by the composition and structure of the material. As discussed in section 3.3.1 there has been a great deal of work looking at the development of amorphous Indium Gallium Zinc Oxide (a-IGZO) as a semiconducting material, through a variety of deposition methods. These include pulsed laser deposition (PLD) [2, 471], chemical solution processing [472–474], atomic layer deposition (ALD) [164], and most commonly sputtering [15, 126, 151, 221, 472, 475, 476]. This previous work is primarily aimed at the used of a-IGZO as the active layer in pixel driving devices for large area displays [2, 145, 155, 172, 184, 477]. As such application is largely based on glass substrates, development has generally used the large thermal budget available to optimise the properties of the a-IGZO, for example through high temperature thermal annealing [15, 478]. It has been shown that these high temperature annealing steps have a positive impact on the device performance.

Electrical characterisation (I-V measurements, discussed in chapter 5) has shown increased field-effect mobility (μ_{FE}) [141, 475, 479, 480] with decreased sub-threshold swing (SS) [479, 481], primarily due to improvements to the semiconducting material itself (in the channel region), and improved device stability, characterised

by reduced hysteresis, due to improvements in the channel/gate dielectric interface [15, 141, 221, 269, 474] For further discussion of these characteristics, and their relation to material structure, see chapter 2.

The mechanisms for these improvements have been theoretically studied through *ab initio* calculations using molecular dynamics and density functional theory, looking at both the isolated semiconducting channel and the channel/gate dielectric interface [482–484]. This has shown that when the channel region contains oxygen vacancies, these act as charge trapping sites causing both a reduction in mobility and an increase in sub-threshold swing [485]. Structural relaxation, facilitated by annealing, may then allow these vacancies to either migrate towards indium atoms [219], or combine with under-coordinated oxygen atoms to create a stoichiometric local environment [486]. It has also been shown that truly stoichiometric channel/gate insulator interfaces do not show any trapping sites, but that the introduction of defects at this interface induces charge trapping [183], the primary cause of hysteresis and device instability, discussed in chapter 2 [155, 487]. These sites trap electrons at the interface, causing a negative shift in the turn-on and threshold voltages, dependent on the amount of trapping. Trapping can be either long term stable, with the electrons trapped when a positive gate bias is applied, shifting the transfer characteristics permanently, or transient, with electrons becoming trapped during positive gate bias and then released, or detrapped, when the bias is reversed, causing transient shielding of the gate that leads to hysteresis between forward and reverse sweeps. As these effects are cycled, charge trapping increases until devices no longer show switching behaviour. The effect of this charge trapping is shown to be significantly reduced following annealing [27, 183].

In addition to providing insight into the mechanisms for device degradation caused by oxygen vacancies within the material and at interfaces, *ab initio* work has shown a strong link between material density and electrical performance [141, 224, 475]. In studies of both the channel and the interface, the presence of oxygen vacancies was shown to be accompanied by metal-metal bonds. It has been found in such material simulations, that the density of metal-metal bonds increases as the density of the material is reduced [183]. This supports numerous experimental studies in which increases in material density have been correlated to improvements in device performance, commonly achieved through

variations in deposition parameters [488–490]. This connection between material density, defect density, and ultimately electronic behaviour makes optimisation of material density an effective route to improving device performance.

The effects of high temperature annealing, >300 °C, on the electronic properties, and on material structure, have been significantly studied [15, 126, 127], however the impact of low- and intermediate-temperature annealing (<300 °C) has received little attention, particularly with regard to the effect of length of time, as well as temperature. This is of particular importance here as the flexible polymer materials used as substrates in the application of this work, are only stable at these low and intermediate temperatures, as discussed in section 3.3.2.3.

Finally it should be noted that the crystallization behaviour of a-IGZO has been well studied elsewhere, and the onset of crystallization does not occur until between 520 °C and 650 °C (depending on stoichiometry, deposition conditions and methods, and multiple other factors) [126, 127], therefore it is reasonable to assume that no crystallisation will occur within the temperature range considered here.

8.1 Experimental details for the systematic study of the annealing of a-IGZO

For investigation of the effects of thermal annealing treatments that are compatible with plastic substrates, 20 nm a-IGZO films were prepared by sputtering. See section 4.1.1 for details of the sputtering process. The base pressure of the sputter system was 0.0666 mPa and the working gas was an argon and oxygen mixture (5% oxygen) that was introduced at 90 sccm with a working pressure of 266.6 mPa.

The material was deposited on single crystal silicon with a native oxide as an analogue of the true device stack. Silicon is used here as the substrate to improve measurement quality while keeping conditions as close as possible to the fabrication process. This arises as, in devices, a-IGZO is deposited on top of the buffer, discussed in the previous chapter, which acts to create a smooth, chemically inert surface, and prevents ingress of moisture from the plastic substrate [52, 491]. This buffer layer, however, adds a significant level of complexity to the XRR data by adding a second set of Keissig fringes

on top of those created by the a-IGZO layer (see for example figure 9.1 in the following chapter, and see section 5.1 for further discussion of Keissig fringes in XRR data). While good fitting can still be achieved with this added complexity, to ensure a-IGZO fitting is as robust as possible, the buffer is removed for this investigation. However, as the plastic substrate underneath the buffer has a relatively high surface roughness and moisture content, the removal of the buffer means that a-IGZO deposited directly onto the plastic would be significantly different from that deposited on the buffer material. Instead, a-IGZO was deposited on silicon, giving clear XRR data used to determine material structure, while keeping conditions close to the full fabrication process. Although the buffer was removed from the sample stack for this study, the interface between a-IGZO and the buffer layer is studied in chapter 9. The samples were annealed in ambient atmospheric conditions at four annealing temperatures, T_{ann}: 150 °C, 200 °C, 250 °C, and 300 °C, with annealing times, t_{ann}, between 1 hour and 36 hours.

Compositional analysis of the as-deposited samples was performed using X-ray photoelectron spectroscopy (XPS) carried out at Kratos Analytical Ltd. For this analysis samples were first cleaned using an argon ion-cluster beam mill, intended to remove residual hydrocarbon contamination from the sample surface by preferentially sputtering the hydrocarbons.

8.2 Results of XPS analysis of deposited a-IGZO

XPS analysis of the deposited a-IGZO was carried out by Kratos Analytical Ltd. Results of this analysis are presented in table 8.1 with the analysis performed after the samples received an argon ion-cluster mill to remove surface contaminants. The atomic composition measured here was used as the film composition in all XRR analysis carried out below. However, it should be noted that this analysis should not be considered definitive as little information was provided by Kratos with regard to either the argon ion milling or the compositionional analysis performed (particularly significant in consideration of the oxygen content of the film, see for example Watts & Wolstenholme for more information on XPS fitting [492]). This lack of detail means that, while the quoted uncertainties are representative of the spread of the reported data, the accuracy of

Table 8.1: Atomic percentage of each element present in 4 samples of a-IGZO after argon ion-cluster beam cleaning (normalised to the level of indium in brackets). Data extracted from XPS measurements performed and fitted by Kratos Analytical Ltd.

Sample	In	Ga	Zn	O	C
1	15.8 (1)	18.5 (1.17)	14.3 (0.91)	48.8 (3.09)	2.6 (0.16)
2	16.1 (1)	19.1 (1.19)	14.7 (0.91)	48.4 (3.01)	1.7 (0.11)
3	15.9 (1)	18.8 (1.18)	14.8 (0.93)	48.5 (3.05)	1.9 (0.12)
4	15.6 (1)	18.3 (1.17)	14.6 (0.94)	47.9 (3.07)	3.5 (0.22)
Average	**15.9±0.2 (1.00±0.01)**	**18.7±0.4 (1.18±0.01)**	**14.6±0.2 (0.92±0.01)**	**48.4±0.4 (3.05±0.04)**	**2.4±0.8 (0.15±0.05)**

these data cannot be assessed independently.

8.3 Fitting of XRR data for annealed a-IGZO

Figure 8.1 shows example XRR data obtained for samples annealed between 150 °C and 300 °C for 1 hour, alongside the data for a sample with no annealing. This data illustrates well the need for good fitting of models to the data as, on visual inspection, there are only very small differences in fringe patterns, and almost no difference in the critical angle.
In previous chapters, looking at aluminium oxide deposited by sputtering and atomic layer deposition, it was found that muli-layer models were needed to accurately fit the XRR data. However, with the a-IGZO deposited here it was found that a multilayer model is unnecessary as a single layer fits the data well. Figure 8.2 shows a comparison of one, two, and three layer models fitted to the same data, were it can be seen that little improvement is seen by introducing more layers. As the improvement in fitting is minimal, for this work a single layer model was used in all instances.

8.4 Results of XRR fitting for annealed a-IGZO

Figure 8.1 also shows the best fitting models from GenX superimposed on the measured data. Here it can be seen that the models and data are in very close agreement for all samples, and is representative of all the fitting performed in this study. The critical angles, θ_c - the first point at which the intensity rapidly decreases, is directly related

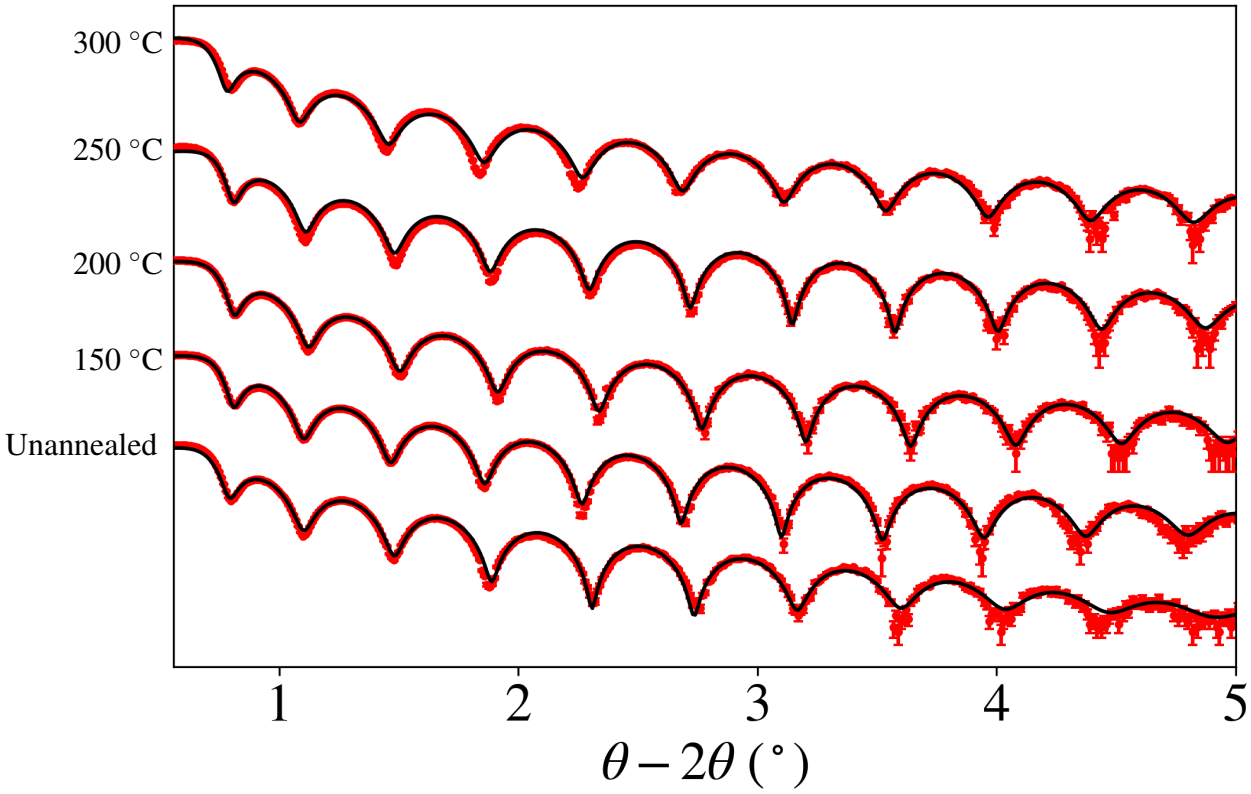


Figure 8.1: XRR data and best fitting models for a-IGZO samples annealed between 150 °C and 300 °C for 1 hour, along with the same data for an unannealed sample. Data is artificially offset in the y-axis for clarity.

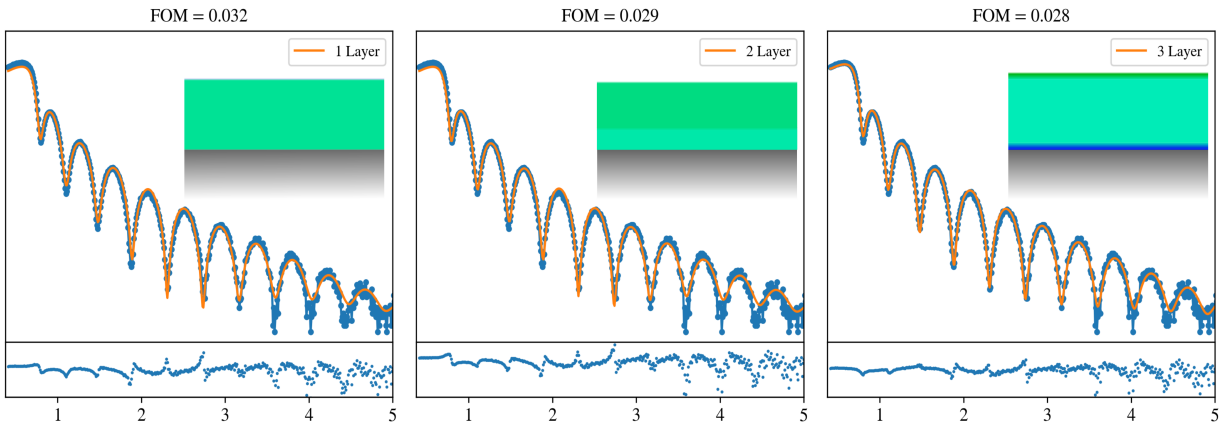


Figure 8.2: Fitting of 1, 2, and 3 layer models to the same XRR data for an unannealed 20 nm a-IGZO layer. Inset is a graphical depiction of the layer structures to scale, with variation in layer density represented by the colour. There is little difference in the residuals and only a small improvement in FOM with increasing number of layers.

to the density of the a-IGZO film, as described in section 5.1, while the spacing of the Kiessig fringes gives a measure of the film thickness, and the rate of attenuation of the signal with angle (above this normal $\sin^4\theta$ attenuation seen) relates to the structure of the film surfaces (the combined width of topological roughness and chemical grading between the sample and air) and the SiO_2-IGZO interfaces [427]. Figures 8.3 shows linear intensity plots around the critical angle from the best fitting model that pertain to samples annealed at 200 °C.

The positive shift in θ_c, seen for anneal times between 0 and 3 hours, shows an increase in the IGZO density, while the negative shift in θ_c for t_{ann}>3 hours indicates a reduction in density.

The best fitting simulations of the XRR data, examples of which are seen in figure 8.3, showed no significant variation in either surface structure width, with an average value of 4.4±0.8 Å (red in figure 8.4), or SiO_2-IGZO interface width with an average value of 1.3±0.7 Å (green in figure 8.4), for all combinations of t_{ann} and T_{ann}. This shows that these interfaces are unaffected by annealing within the temperature range studied here. Similarly, for most temperatures studied here there is little change in thickness of the material with annealing time, blue figure 8.4.

The final measure of material structure, the density, is the only parameter to show significant changes under all conditions investigated. Data for the density of these a-IGZO samples with annealing is presented in figure 8.5, with analysis of this in the following sections.

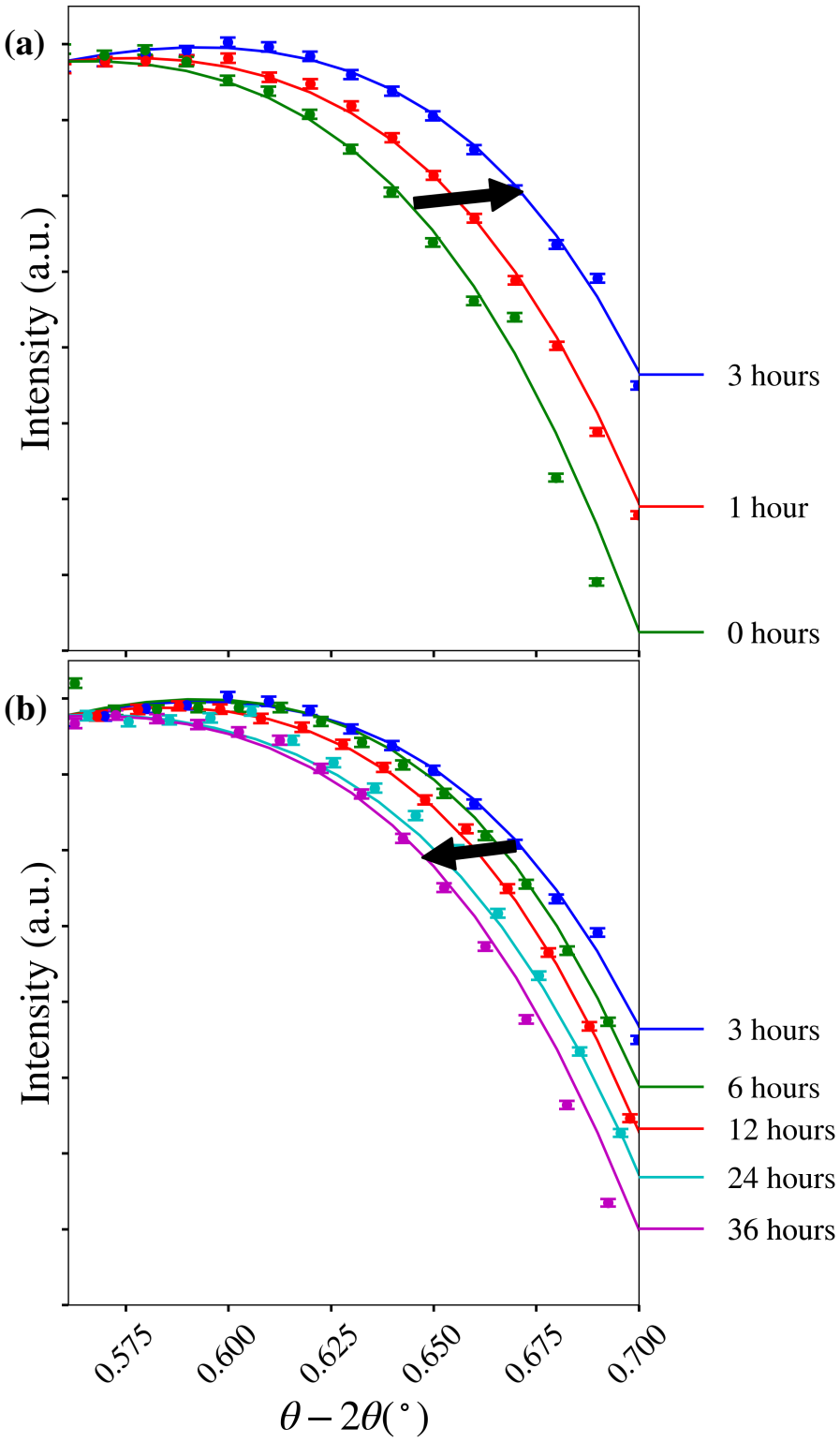


Figure 8.3: **(a)** and **(b)** show the XRR fits for samples annealed at 200 °C from 0 to 36 hours. **(a)** From 0 to 3 hours there is a positive shift in the critical angle, while **(b)** from 3 to 36 hours there is a negative shift in the critical angle.

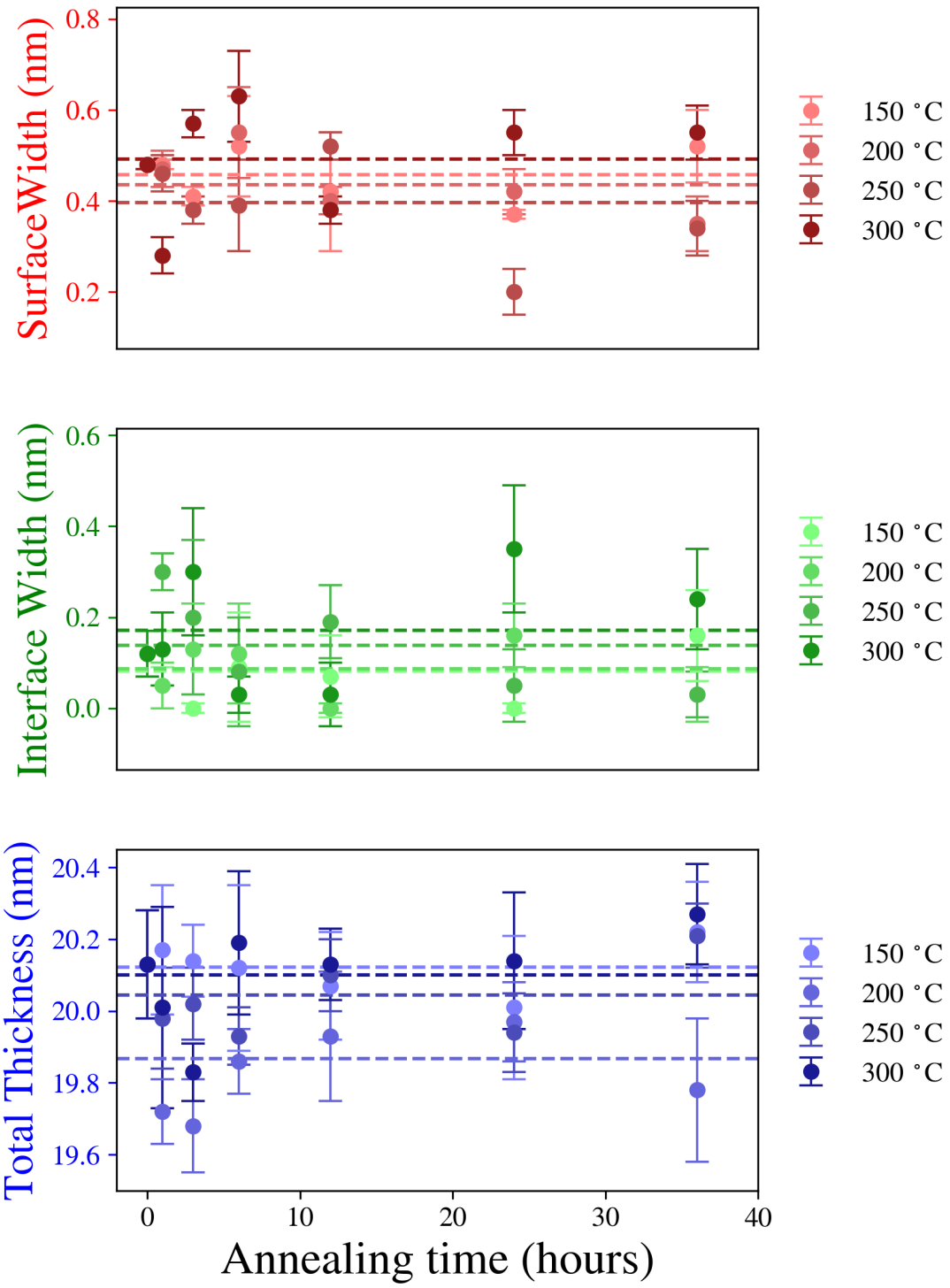


Figure 8.4: Surface width (red), back interface width (green), and total film thickness (blue) of a-IGZO annealed at different temperatures up to 36 hours, extracted from best fitting models for XRR data. Dotted lines represent the average width at each temperature.

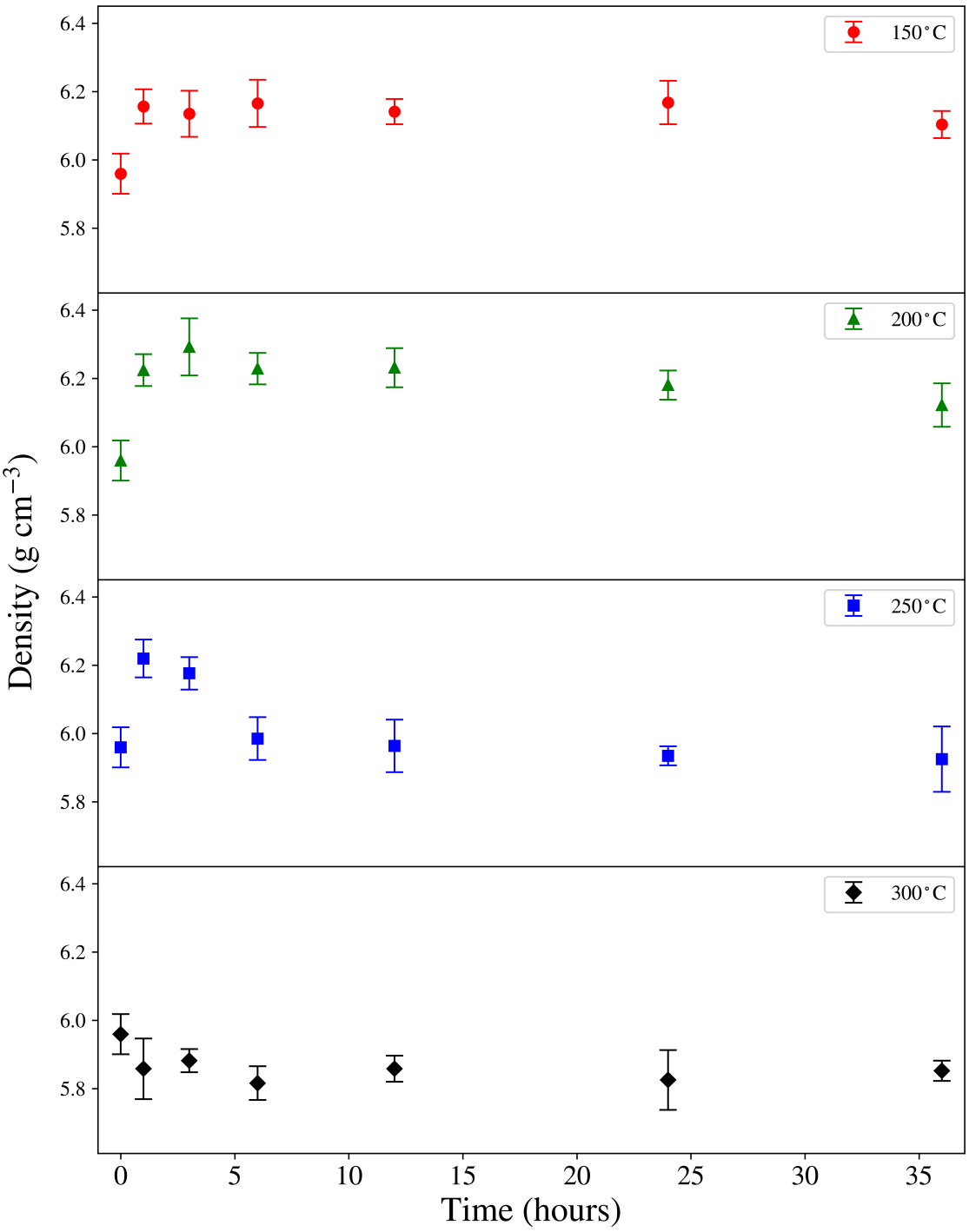


Figure 8.5: Density of a-IGZO annealed at different temperatures up to 36 hours, extracted from best fitting models for XRR data.

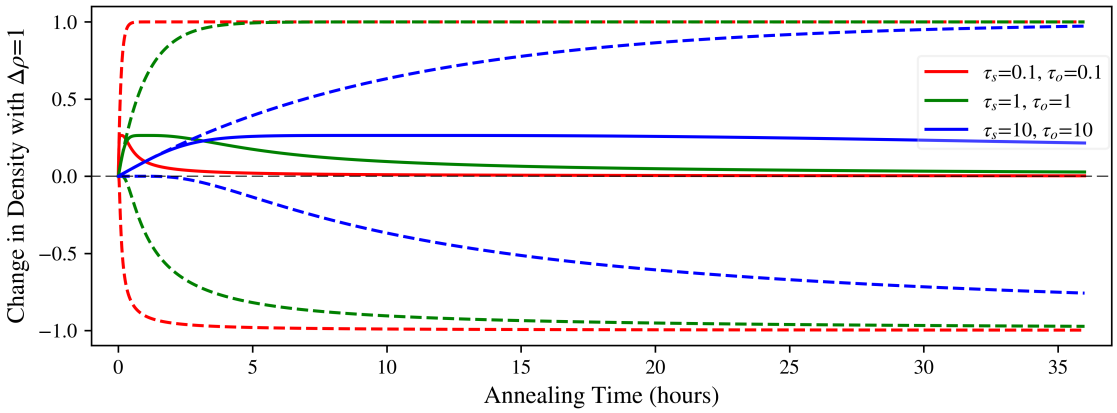
8.5 A semi-empirical model for the change in density of a-IGZO with annealing time

In the figure 8.5 it can be seen that, for temperatures up to 250 °C, the density of the a-IGZO films, extracted from best fitting models for the XRR data, shows an initial sharp rise, followed by a slow fall. In contrast, for samples annealed at 300 °C this initial increase in density is not present. The dependence of the density on annealing has been interpreted in terms of a thermal activation model with two thermally activated component processes. These two processes, which act antagonistically, are represented by an initial exponential, as proposed by Moynihan et al. for the densification of amorphous solids by structural relaxation [493, 494]. and a more delayed exponential reduction in density at longer anneal times that is attributed here to the absorption of oxygen. These two processes are combined in the form

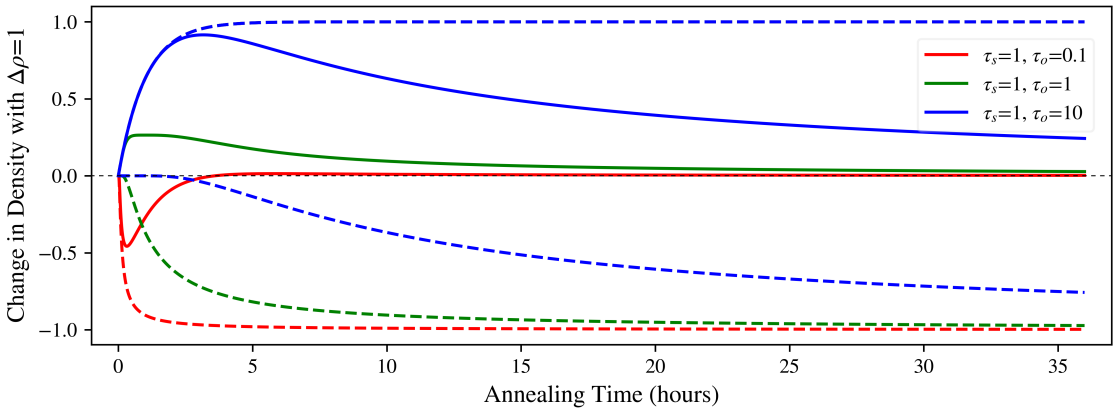
$$\rho(t) = \Delta\rho_s \left(1 - \exp\left[\frac{-t}{\tau_s}\right]\right) - \Delta\rho_o \exp\left[\frac{-\tau_o}{t}\right] + \rho_0 \tag{8.5.1}$$

where $\rho(t)$ is the density as a function of annealing time t, ρ_0 is the initial material density, $\Delta\rho_s$ is the change in density due to structural relaxation, τ_s the characteristic time for structural relaxation, $\Delta\rho_o$ is the change in density due to oxygen absorption, and τ_o the characteristic time for this oxygen absorption. The effects of these two components individually, as well as their combined effects, are illustrated in figure 8.6 for ρ_0=0 with $\Delta\rho_s$ and $\Delta\rho_o$ set to 1 for illustration.

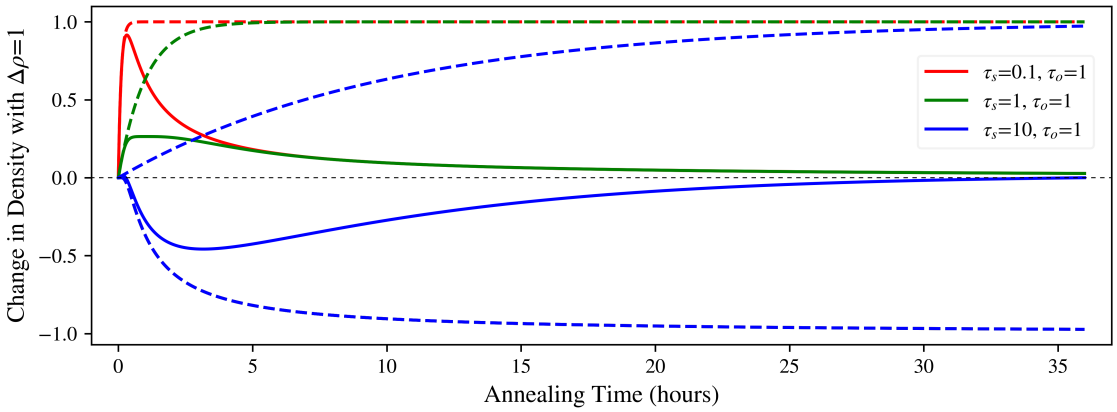
As can be seen in figure 8.6, the different values of τ determine how much material increases or decreases in density, both for shorter and longer annealing times. What should be noted is the delayed onset of the second (negative) term in equation 8.5.1. This delay in the negative term is more pronounced at higher values of τ_o, but is also present (although hard to distinguish) at lower values of τ_o. Implications of this delayed onset will be considered below.



(a) Effect of varying τ_s and τ_o at the same time with the same values.



(b) Effect of varying τ_o while holding τ_s at 1.



(c) Effect of varying τ_s while holding τ_o at 1.

Figure 8.6: Illustrations of the effect of changing τ_s and τ_o in equation 8.5.1 while holding $\Delta\rho_s$ and $\Delta\rho_o$ at 1. The positive dashed line represents the densification through structural relaxation term, the negative dashed line represents decrease in density due to oxygen absorption, and the solid line is the combined effect.

8.6 Analysis of change in density in annealed a-IGZO

Figure 8.7 shows the density of the a-IGZO films as a function of their annealing time with equation 8.5.1 fitted to the data using least squares methods. It can be seen that the function proposed in the previous section fits the data here well, suggesting that the model is suitable to this work. Figure 8.8 shows the same fitting as 8.7 but with the two components of equation 8.5.1, that contribute to the fitting, overlayed as dotted lines. From this it is clear that the magnitude of both components increases with temperature, and that they proceed more rapidly as temperature increases. This is confirmed in figure 8.9, where the $\Delta\rho$ parameters increase with temperature, indicating greater contribution from each component, and the τ parameters decrease with temperature, indicating a shorter characteristic time for the mechanisms to take effect. The term ρ_0 has not been included in this figure as the fitting process showed little variation, as can be seen in table 8.2 in which all of these extracted parameter values are presented. This fits well with expectation as the term is attributed to the density of material before annealing, which was the same for all samples, and provides more confidence in the validity of the model. As well as illustrating trends with annealing temperature, figure 8.9 helps with understanding of the relative contribution of each component of the model to the fitting. For example it is clear that there is a difference in behaviour of the structural relaxation term, compared to oxygen absorption, with regards to temperature. While the fall in characteristic time for structural relaxation, τ_s, appears nearly linear with temperature, there is only a small change in the characteristic time for oxygen absorption, τ_o, between 150 °C and 200 °C, followed by a linear reduction at a higher temperatures. Similarly for the size of these effects, while the magnitude of the structural relaxation term, $\Delta\rho_s$, increases a small amount between 150 °C and 200 °C followed by a more rapid increase above this, the magnitude of the oxygen absorption term does not increase at all between 150 °C and 200 °C, after which the increase is more pronounced than that for structural relaxation.

All of these effects can be considered within the frame of thermal activation energies, using an Arrhenius type equation and plotting $1/\tau$ (the equivalent of the rate constant) against the absolute temperature [495, 496]. Figure 8.10 shows these values along with a

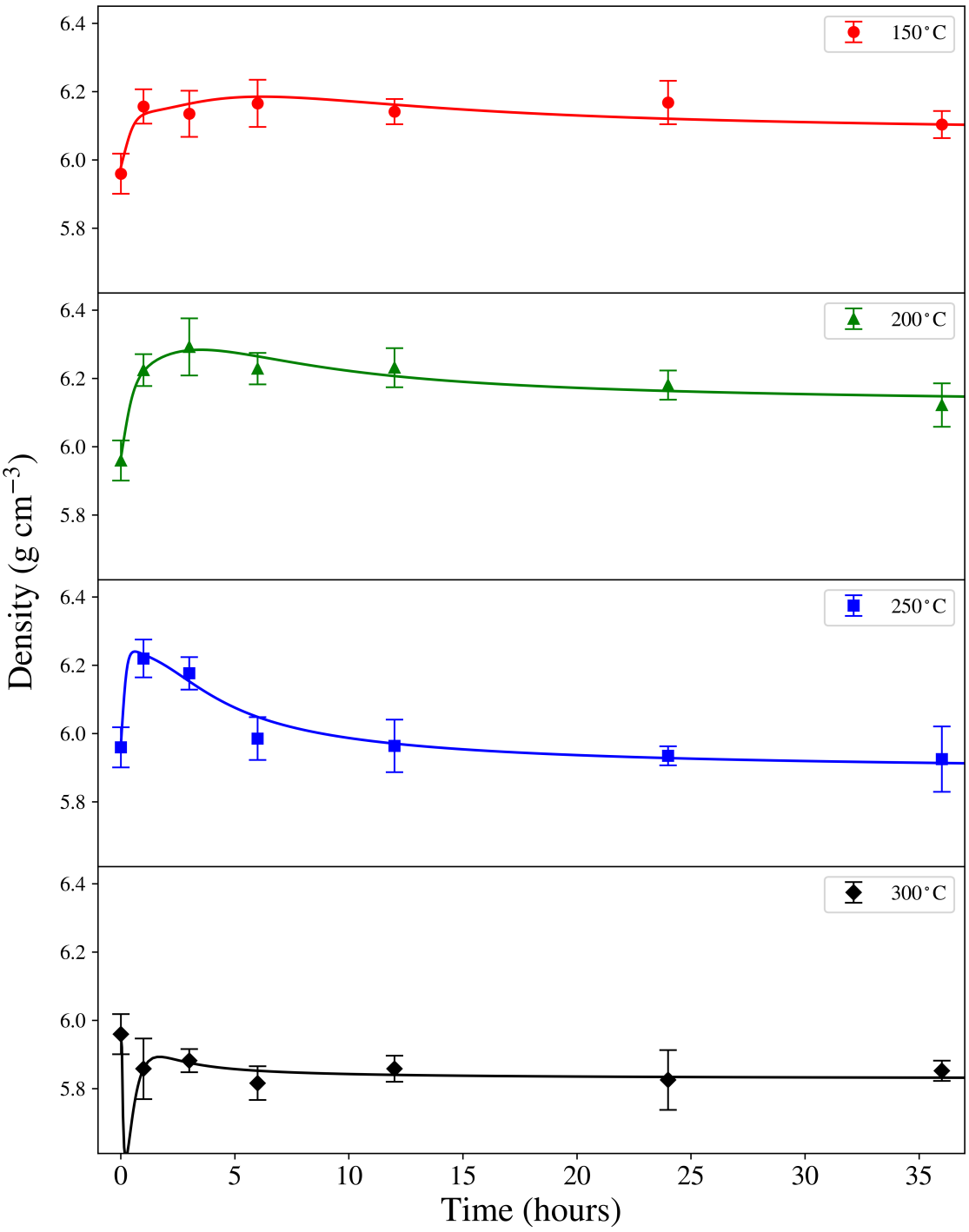


Figure 8.7: Density of a-IGZO annealed at different temperatures, as depicted in figure 8.5, with equation 8.5.1 fitted, via least squares fitting methods, to the data.

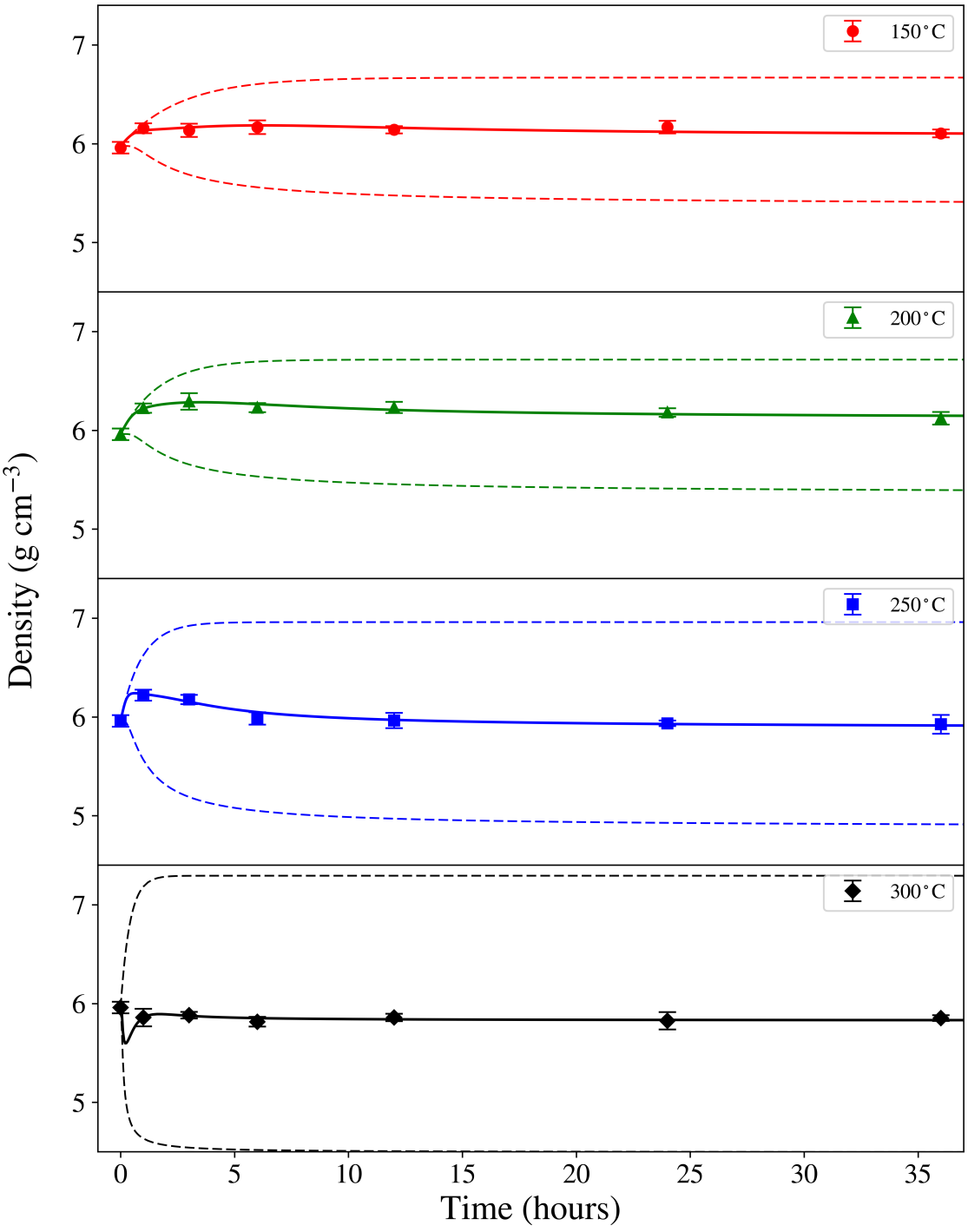


Figure 8.8: Density of a-IGZO annealed at different temperatures, as depicted in figure 8.5, with equation 8.5.1 fitted, via least squares fitting methods, to the data. The component parts of the equation are shown as dotted lines as corresponding to the illustrations of the equation presented in figure 8.6.

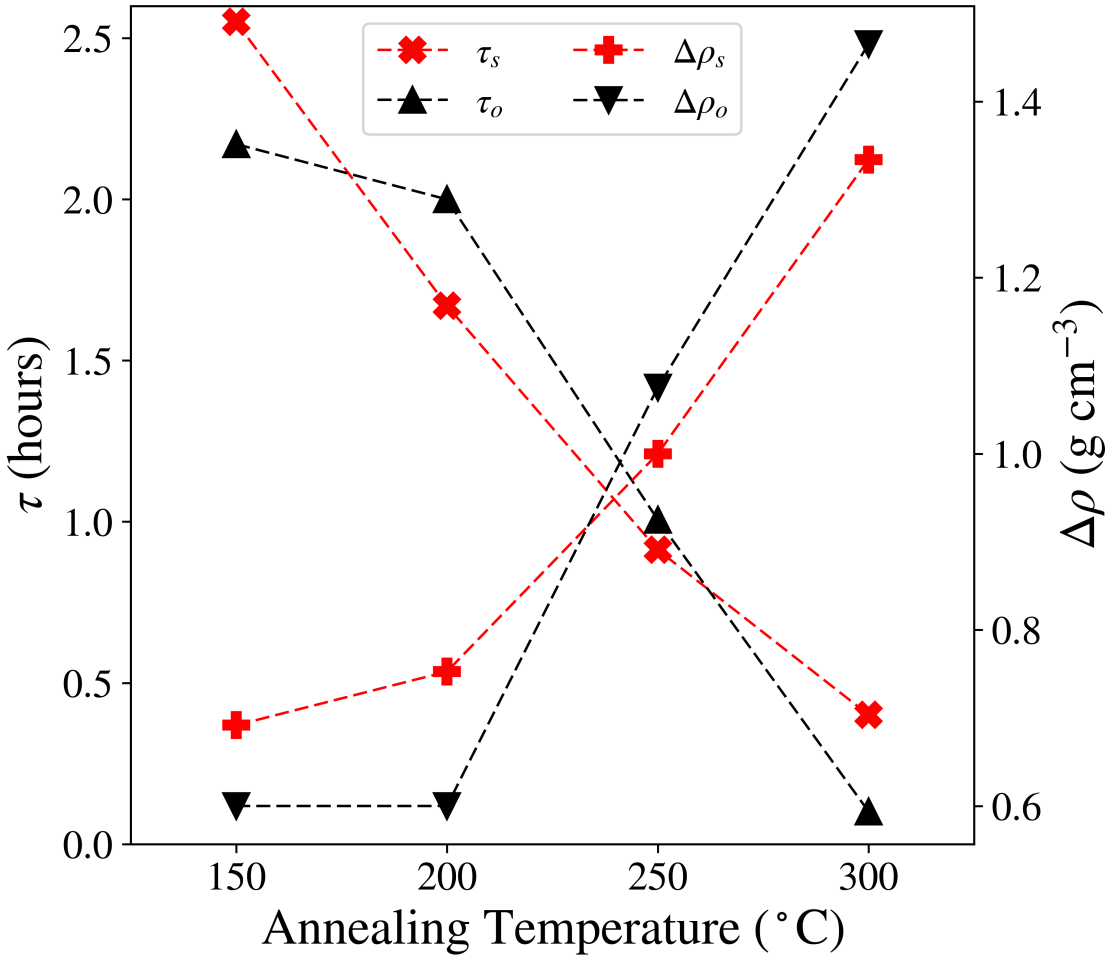


Figure 8.9: The value for each variable in equation 8.5.1 when fitted to the density of a-IGZO films after annealing for various times up to 36 hours, from the best fitting model for the XRR data. Parameters associated with structural relaxation are shown in red, and oxygen absorption in black.

Table 8.2: Parameters of equation 8.5.1 fitted to the density of a-IGZO with annealing, as shown in figure 8.7.

Temperature (°C)	τ_s (hours)	$\Delta\rho_s$ (g cm^{-}3)	τ_0 (hours)	$\Delta\rho_o$ (g cm^{-}3)	ρ_0 (g cm^{-}3)
150	2.55	0.69	2.17	0.60	5.98
200	1.67	0.75	2.00	0.60	5.96
250	0.91	1.00	1.01	1.08	5.96
300	0.40	1.33	0.10	1.47	5.96

fit of an Arrhenius type equation of the form

$$\frac{1}{\tau} = Ae^{\frac{-E_a}{k_B T}} + C \tag{8.6.2}$$

where A is a pre-exponential factor, E_a is the activation energy barrier, k_B is Boltzmann's constant, T is the absolute temperature, and C is a constant offset.

The form of this equation is taken from the standard application of the Arrhenius equation to solid systems, considering the energy per molecule, with a constant offset, C, indicating non-thermally activated processes alongside the thermal processes here. From the fitting of this equation, show in figure 8.10, the activation energy, E_a, for each process (structural relaxation and oxygen absorption) is extracted as 531 meV and 1423 meV respectively. The difference in these activation energies, therefore, can explain why structural relaxation is dominant at shorter annealing times. Since the processes are controlled by Boltzmann statistics, at any given time sufficient energy will only be available to over come the energy barrier to a process in a few instances. As the thermal energy increases, the proportion of the population with sufficient energy to overcome the energy barrier increases. Where the energy barrier is high, when $E_a >> k_B T$, this population is negligible. However, when $k_B T$ approaches E_a the population rises quickly. In this instance, where the energy barrier for structural relaxation is significantly lower than that for oxygen absorption, the relaxation is able to proceed more rapidly and becomes dominant at short annealing times. As annealing continues, however, structural relaxation quickly plateaus (as seen in figure 8.8), and oxygen absorption becomes more apparent. This, then, explains the apparent lack of densification in samples annealed at 300 °C as enough thermal energy is present to allow both structural relaxation and oxygen absorption to undergo the majority of their action in less that 1 hour (the shortest annealing time investigated here).

This thermal activation model can be further extended to explain the changes in the magnitude of each component with temperature, by considering the limitation of the Arrhenius model in general. Arrhenius' equation is a semi-empirical model conceived of for atomistic reactions, meaning only a single thermal barrier in be considered. With the system under consideration here, however, it is expected that many different mechanisms exist with varying activation energy barriers. These include elemental and vacancy

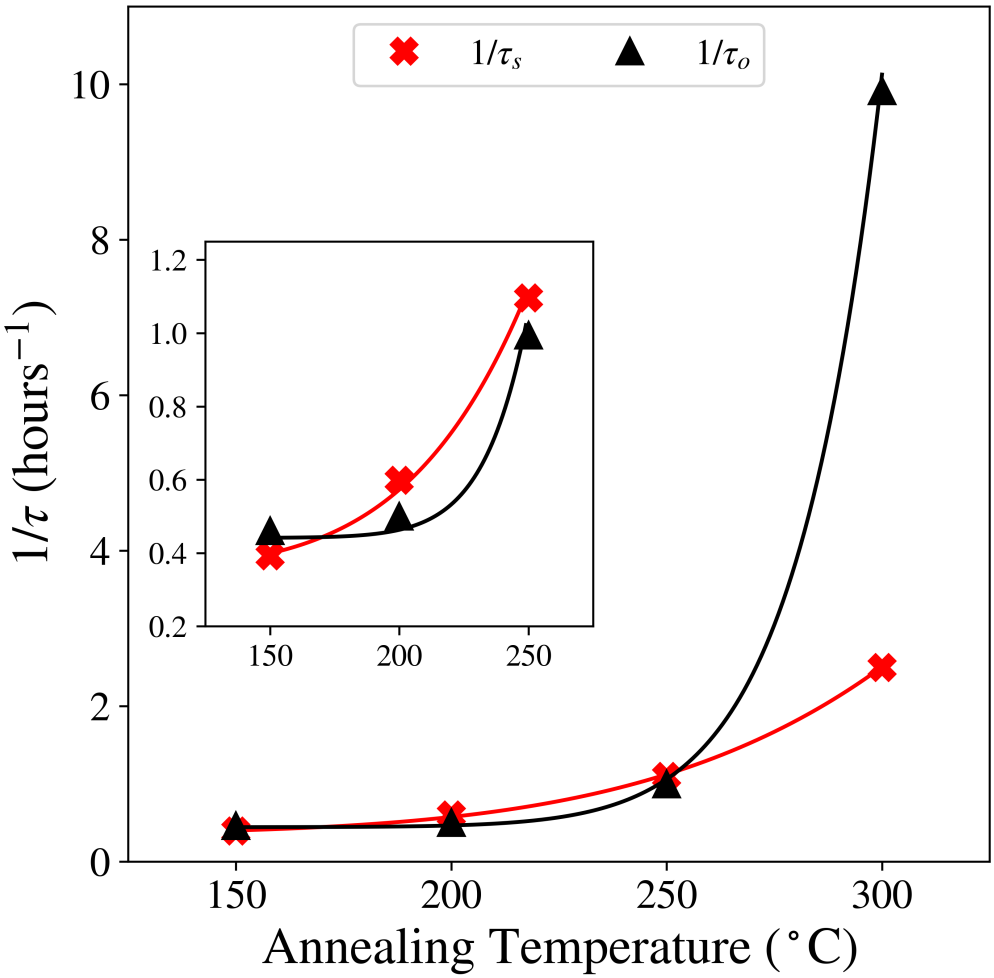


Figure 8.10: Inverse of the characteristic times $(1/\tau)$ for τ_s and τ_o fitted with the Arrhenius type function, equation 8.6.2. Inset: The same data, limited to 250 °C to make the behaviour and fitting < 300°C clearer.

migration though the material, particularly migration of oxygen atoms and vacancies, the energy barrier for which is dependent on the nearest neighbour species, and bond breaking and making as local non-stoichiometries are resolved, again dependent on the species being considered. The energy barriers, extracted from the fitting in figure 8.10, are therefore just the average value for the myriad different energy barriers contributing to each component. This means there are some mechanisms with low energy barriers which likely contribute more significantly at lower annealing temperatures and times, while there are others with higher barriers that are overcome only at higher temperatures and longer times. Because of this, each component of the density equation, 8.5.1, increases in the size of its contribution as annealing temperature rises since more and more of these energy barriers are overcome.

Finally, the change in density due to these components can provide insight as to why little change in thickness is observed with the changing density. The structural relaxation term in equation 8.5.1 is presented here as true densification of the a-IGZO film, i.e. the film becomes more dense as the structure of the film is allowed to relax into an energy minimum. This implies no chance in the composition of the film, and therefore no change in mass. As the film is constrained in the in-plane dimensions (the width and length of the film), any change in density must, therefore, correspond to a change in thickness of the film. This expected change in thickness can be estimated from the change in density, $\Delta\rho_s$, as:

$$\Delta T = k\Delta\rho_s \tag{8.6.3}$$

where ΔT is the change in thickness and k is a constant of proportionality described as

$$k = \frac{1}{m/LW} \tag{8.6.4}$$

m being mass, and L and W being the in-plane length and width. This can, in turn, be calculated from the original density, ρ_0, and thickness, T_0, as

$$\rho_0 = \frac{m}{LW} \cdot \frac{1}{T_0} \tag{8.6.5}$$

meaning, finally, that the expected change in thickness due to structural relaxation can be calculated as

$$\Delta T = \rho_0 T_0 \Delta\rho_s \tag{8.6.6}$$

Taking this equation, with the values for $\Delta\rho_s$ presented in table 8.2, expected changes in thickness of between 2.32 nm and 4.49 nm can be calculated. However, as the second term in equation 8.5.1, acts antagonistically, to reduce the apparent density of the films, this is not seen. Here, however, we do not get straightforward reduction in density due to rarefication of the film (i.e. the atoms in the film simply moving further apart). Instead, oxygen is absorbed into the film, changing the atomic composition. The change in composition provides several routes to changing the measured density of the film: firstly the incorporation of more oxygen means, as metal-metal bonds are broken in favour of the formation of metal-oxygen bonds, there is outward structural relaxation as the oxygen-metal bond lengths are generally longer. Secondly, the incorporation of more atoms within the film means the existing atoms relax outward to accommodate the new atoms. And finally, the change in composition also alters the electron density of the film, which is what is truly measured through XRR measurements, thereby distorting the value of density extracted from the XRR model due to the now unknown sample composition. All three of these effects have varying and complex contributions to the film's density and thickness, which have not been explored further here due to time and resource constraints. However, this does warrant further investigation in the future, specifically though the systematic study of film composition and structure, preferably simultaneously *in situ* during annealing using a synchrotron light source to perform complementary XPS and XRR measurements.

8.7 Implementation of beneficial annealing step in production devices

Following the above analysis, an anneal of 1 hour at 200 °C was trialed in full TFT manufacturing. This time/temperature combination was chosen so as to provide maximum structural relaxation with minimum oxygen absorption, thereby increasing device performance (as discussed at the start of this chapter) without sacrificing carrier density by removing oxygen vacancies (which act as shallow donors). Devices with multiple channel width:length ratios where fabricated, with the anneal taking place after deposition of the IGZO and before any further processing. After performing I-V

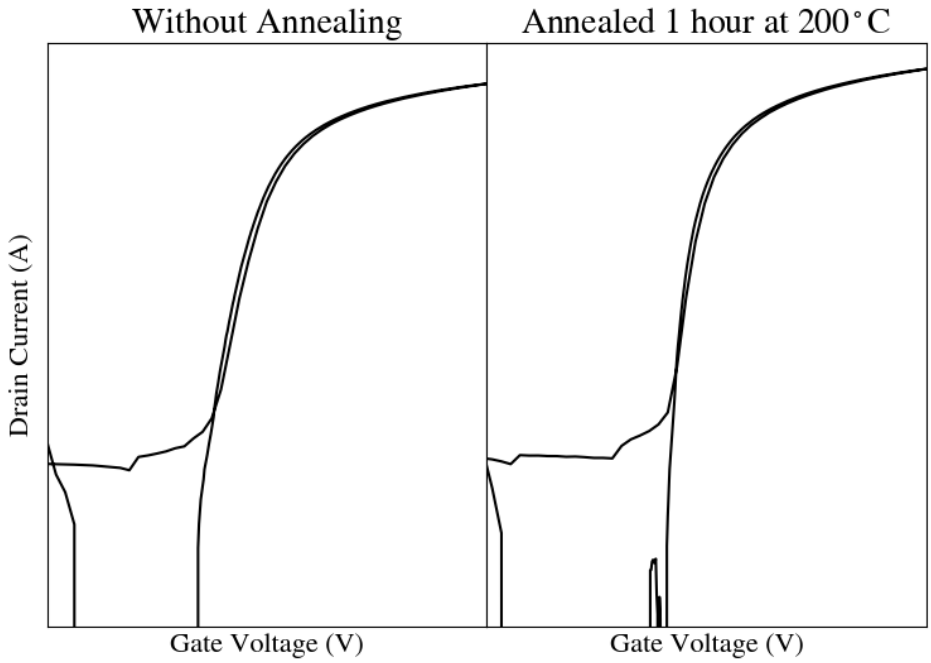


Figure 8.11: Representative IV curves for devices fabricated with and without a 1 hour anneal at 200° after deposition of the a-IGZO layer. Curves shown are representative curves taken from devices with channel length of 10 μm and channel width of 1 μm.

transfer sweeps between -6 V and +6 V, it was found that devices which received this anneal step, when compared to identical devices made without the anneal step, showed significant improvement in multiple device characteristics, consistent with the reduction of defects in the a-IGZO channel and interface. These improvements are summarised in table 8.3, while figure 8.11 exemplifies this with representative transfer curves for 10×1 μm (Width$\times$Length) devices fabricated with and without the annealing step. It is seen here that there is improvement in all of these parameters, with the annealed devices showing higher mobility and switching ratio, and lower subthreshold swing and hysteresis. It was also found, however, that there was a negative shift in both V_{on} and V_{th} after the introduction of the annealing step. The magnitude of this shift appears to be dependent on the channel widths, and was found to be $\Delta V_{on} = -0.26 \pm 0.05$ and $\Delta V_{th} = -0.36 \pm 0.14$ for devices with a width of 10 μm. This negative shift in V_{on} and V_{th} implies an increase in trapping sites at the a-IGZO to gate dielectric interface, not considered in this study but further investigated later in the following chapter.

Table 8.3: Changes in device characteristics between annealed and unannealed devices. Figures quoted are averaged over devices with multiple channel length:width ratios. I-V sweeps where carried out between -6 V and +6 V in a forward and reverse directions, and the parameter values extracted from these curves.

Parameter	Positive Sweep	Negative Sweep
μ_{FE}	+17.3%	+26.8%
$\mathbf{I}_{on/off}$	+433%	+519%
SS	-29.5%	-16.0%
Hysteresis	-45.3%	

8.8 Conclusions

In summary, a detailed systematic structural and compositional study of amorphous InGaZnO as a function of time at relatively low annealing temperatures was undertaken. The results show that the density of a-IGZO can be increased through short term annealing, and that longer term annealing then causes a reduction in material density. This change in density is interpreted as being due to two competing mechanisms; the structural relaxation of the amorphous phase, and oxygen absorption. Fitting of the experimental data to the model presented indicates that structural relaxation has a more dominant effect at lower temperatures and shorter times, and that oxygen absorption has a greater impact on material density as these are increased. These mechanisms are considered to be thermally activated processes with the dependence on both time and temperature, interpreted as being due to differing energy barrier heights. Average energy barriers for structural relaxation and oxygen absorption are found to be 531 meV and 1423 meV respectively, extracted from fitting of an Arrhenius type equation to the characteristic times for each process. It is further proposed that a range of energy barriers exist for each mechanism, evidenced by the dependence of the magnitude of each mechanism on temperature. The values for the energy barriers obtained here are for material that is initially oxygen depleted, requiring around one oxygen per "unit cell" to achieve conventional stoichiometry, suggesting the energy requirements are likely to change for other stoichiometries.

A maximum densification of 5.6% from the as-deposited material was achieved at 200 °C, where structural relaxation is able to proceed, while minimal oxygen is absorbed. In

addition, little change in thickness was observed, but a discussion of expected change in thickness due to structural relaxation is presented. It is expected that this change is thickness is not seen due to the various factors associated with the oxygen absorption process. No work is presented here on trying to understand this, due to limitations of time and resources, but it is suggested that further investigation may help elucidate the mechanics of this mechanism.

Finally it should be noted that, as this study is concerned primarily with the changes in the a-IGZO material, and the absorption of oxygen through the top surface, the conclusions drawn here, although taken from samples produced on a silicon substrate, are applicable to any other flexible or non-flexible substrate. Considered within the realm of a-IGZO TFT fabrication, these results provide strong guidance for mid-process annealing, whereby the density of a-IGZO can be improved, correlated to improved material structure and corresponding improved device performance, without affecting other material layers.

Chapter 9

Studies of the interface between a-IGZO and Al_2O_3

In the devices considered in this work, the semiconducting amorphous Indium Gallium Zinc Oxide (a-IGZO) layer is sandwiched between two layers of aluminium oxide. This means there are two a-IGZO to Al_2O_3 interfaces that may affect device performance. Both of these interfaces have been mentioned in previous chapters, but have not been investigated so far. This chapter presents consideration of these interfaces, exploring first the interface between the buffer material (previously discussed in isolation in chapter 7) and a-IGZO (discussed in isolation in chapter 8), and then the interface between the a-IGZO and the gate dielectric (discussed in chapter 6).

9.1 Differences in interface and layer structure in ALD and sputter deposited Al_2O_3 buffer layers with an a-IGZO cap

Chapter 7 presented an investigation of the structure of aluminium oxide deposited through sputtering and atomic layer deposition (ALD) in an attempt to understand why devices produced with ALD material show degraded electrical performance compared to those produced using sputtered material (data not shown). In that study, some differences in structure where found, but these largely correspond to differences within the bulk

of the layer, rather than at the surface where differences are expected to impact device performance. This section now investigates the structure of the interface between these two forms of buffer material and the semiconducting a-IGZO layer. For this investigation, X-ray reflectivity (XRR) was again employed to probe the buried interface between the two layers.

Al_2O_3 was deposited on single crystal Si wafers with native oxide by either sputtering or ALD processes, with a target thickness of 50 nm. All samples subsequently had a layer of a-IGZO sputter deposited on top of the buffer in the sputter system described in chapter 4. All a-IGZO depositions were carried out in the same run to minimise variation between samples due to process variations. Sputtered Al_2O_3 material was deposited in the sputtering system described in chapter 4, and the ALD Al_2O_3 was deposited in the Beneq TFS500 system, also described in chapter 4, using the optimised conditions from chapter 6.

Samples were measured by XRR in the specular geometry with additional rocking curves measured at the first and second Keissig maxima in order to inform on intermixing and roughness at the interface.

Before considering the interface, consideration of the layer structuring is useful. Figure 9.1 shows typical XRR data for stacks of $\sim$50 nm Al_2O_3 buffer with $\sim$20 nm a-IGZO deposited on top, where the Al_2O_3 was deposited by ALD and by sputtering. The upper, blue data is fitted with a model consisting of just a single layer of Al_2O_3 and a single layer of a-IGZO fitted to it (red line) while the lower, green data has the multilayered models presented in chapters 6 and 7 fitted to it (red line). Below each graph are the statistical residuals for the model fits, in the corresponding colours.

For the ALD Al_2O_3, the fitted models and the data shows little difference between the two different models, although the residuals show significantly more non-random structuring, indicating poorer agreement between the best model and the data for the single layer fit. This is reflected in the figure of merit (FOM) values, with FOM=23.67 for the single layer model and FOM=19.69 for the multilayer model with n=0.001 in the FOM (see section 5.9).

The difference between the fitting of the two models is more significant for the sputtered Al_2O_3, where there is a significant enhancement in the data seen around 3.5°, similar to

Table 9.1: Results of best model fitting to XRR data for buffer/a-IGZO stacks with the buffer layer deposited by either sputtering or ALD.

Parameter	Sputtered Buffer	ALD Buffer
a-IGZO thickness (nm)	17.9±0.2	17.7±0.1
a-IGZO density (g/cm^3)	6.2±0.1	6.2±0.1
a-IGZO surface roughness (nm)	1.42±0.04	0.99±0.03
Al_2O_3 thickness (nm)	52.0±0.5	47.4±0.2
Al_2O_3 density (g/cm^{-3})	3.1±0.1	3.9±0.1
Al_2O_3 interface width (nm)	0.76±0.04	0.59±0.02

that seen in the sputtered material on its own. The single layer model fails to accurately capture this enhancement, as can be seen by examining either the data or the residuals. The multilayer model, with multiple sub-layers corresponding to the movement of the sample past the target in the sputtering system during deposition, captures this enhancement well, providing a more accurate description of the material. This is again reflected in the FOM values, with the single layer model having FOM=48.86 and the multilayer model having FOM=28.82 with the same value of n.

Given the improved fitting of the multilayer models, these were used for the analysis in this work.

9.1.1 Results of XRR examination of the buffer/a-IGZO stack

As the measurement and fitting of rocking curves takes a significant amount of time and computational power, only one measurement of rocking curves was carried out for each sample, although 3 standard XRR measurements were performed (without rocking curves) to establish the layer parameters. The parameters extracted from fitting of these standard measurements are shown in table 9.1 (with errors estimated as the standard deviation across samples with the same stack). These results show some variation between the two stacks in the buffer layer, particularly in the density of the two types of Al_2O_3, with the ALD material showing a higher density than the sputtered material. However, the interface width between the Al_2O_3 and the a-IGZO is very similar and all of the parameters of the a-IGZO are the same within the error margin for the two stacks.

The similarity between the two stacks suggests it is unlikely that any difference in layer

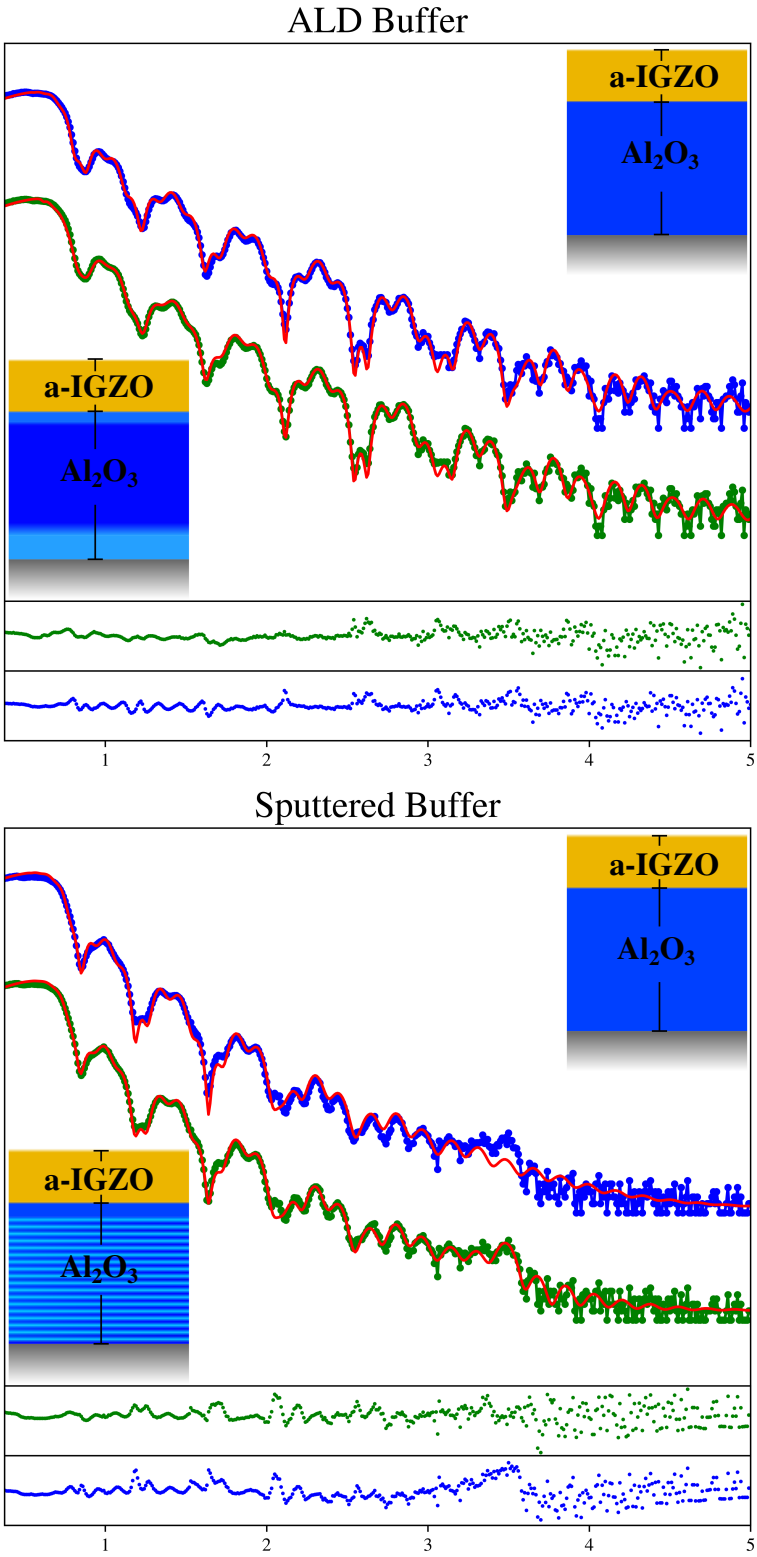


Figure 9.1: XRR data with fitted models for sputtered and ALD deposited buffer layers with the a-IGZO layer on top. Upper data in each plot show the fit for a single layer model of the buffer, the lower data show the fit for multilayer models as described in chapters 7 and 6, these are artificially offset for ease of viewing. Residuals are plotted below in the corresponding colour, and inset are scale schematic representations of the stacks.

structure causes the degraded device performance found with ALD buffer layer. Indeed, the only difference observed here, the increased density of the ALD material, should lead to enhanced performance, as there are fewer trap sites in the buffer to degrade performance.

In a further attempt to find physical differences between the two buffer layer types, XRR rocking curve measurements were taken. These measurements are exemplified in figure 9.2, in which the theta rocking curves are projected onto the 2θ axis, so the peak appears in the correct position on the specular reflectivity curves (see section 5.1). The good fits of the models to the data in figure 9.2 indicates that the results extracted from this model provide a good representation of the interface. Key parameters of these models are summarised in table 9.2. As expected, the surface roughness of the a-IGZO in these models matches that extracted from the models for just the specular reflectivity, giving further confidence in the quality of the other derived parameters.

There are several parameters worth commenting on in this table. First is the topological interface roughness (i.e. how rough the interface is while remaining chemically distinct) between the two samples, and the difference in chemical intermixing at this interface. It can be seen that the roughness is similar for both buffer materials, with the ALD buffer having a marginally higher roughness (0.55 ± 0.04 nm compared to the sputtered material's 0.39 ± 0.04 nm). Conversely, the sputtered buffer shows significantly higher chemical intermixing at the interface. While the absolute values of both the roughness and the intermixing are small (only a few atomic radii in total), the difference in intermixing is significant. It is likely that ALD shows low intermixing due to the chemically complete nature of the deposition, with all chemical bonds made before the deposition of a-IGZO. Sputtering, however, has greater possibility of deposition of material with a non-stoichiometric surface, leaving dangling bonds or excess oxygen [497,498]. If this is the case, the energy of the incident a-IGZO material as it is deposited may be sufficient to allow rearrangement of the atoms at the surface to accommodate these under-coordinated atoms.

The three remaining parameters, ξ, $\xi_\perp$, and H, are global parameters describing the entire sample stack. ξ and $\xi_\perp$ are in-plane and out-of-plane correlation lengths respectively, describing the correlation of roughness in the plane of the sample and between layers. In

Table 9.2: Key additional parameters extracted from best fitting models fitted to specular reflectivity and rocking curves simultaneously. In all cases $\xi_\perp$ reached the physical limit of the model (set at 100 nm) intended to reflect the out-of-plane (z) thickness of the sample.

Parameter	Sputtered Buffer	ALD Buffer
a-IGZO Roughness (nm)	1.42 ± 0.04	1.03 ± 0.04
Interface Roughness (nm)	0.39 ± 0.04	0.55 ± 0.04
Interface Intermixing (nm)	0.54 ± 0.03	0.06 ± 0.10
ξ (nm)	1800 ± 600	2500 ± 700
$\xi_\perp$ (nm)	Limit (100)	Limit (100)
H	0.0016 ± 0.0008	0.0045 ± 0.0019

the fitting of the model, $\xi_\perp$ was limited to 100 nm (slightly greater than the total thickness of the deposited material) as a correlation length greater than this has little physical meaning. Nonetheless in all cases $\xi_\perp$ hit this limit, as indicated in the table. While ξ was not limited in the same way as $\xi_\perp$, it was found that there was significant variation from sample to sample with the same buffer material, as indicated by the large errors associated with these values. The likely cause of these anomalies is the relatively low levels of roughness and high uniformity of this roughness (i.e. the roughness that does exist is highly self-similar on different length scales). The third parameter, H, is known as the jaggedness parameter, and describes how jagged or smooth the roughness is at the interfaces. H takes values between 0 and 1, with higher values describing higher levels of jaggedness. It can be seen that for both buffer materials the value of H is low, but that the ALD buffer is slightly more jagged than the sputtered buffer. This is likely due to similar mechanisms as described above for the intermixing, where the ALD material does not change due to the a-IGZO deposition, but the sputtered material does, thereby smoothing out some of the jaggedness while causing intermixing.

9.1.2 Conclusions on the buffer/semiconductor interface

The study here of the interface between the semiconducting a-IGZO layer and two different forms of buffer Al_2O_3 provides some insight into the structure of this interface. As discussed in previous chapters, Al_2O_3 deposited by ALD and by sputtering shows distinct internal structuring consisting of multiple sub-layers within a single layer of deposited material. However, these sub-layers have little effect on the subsequent

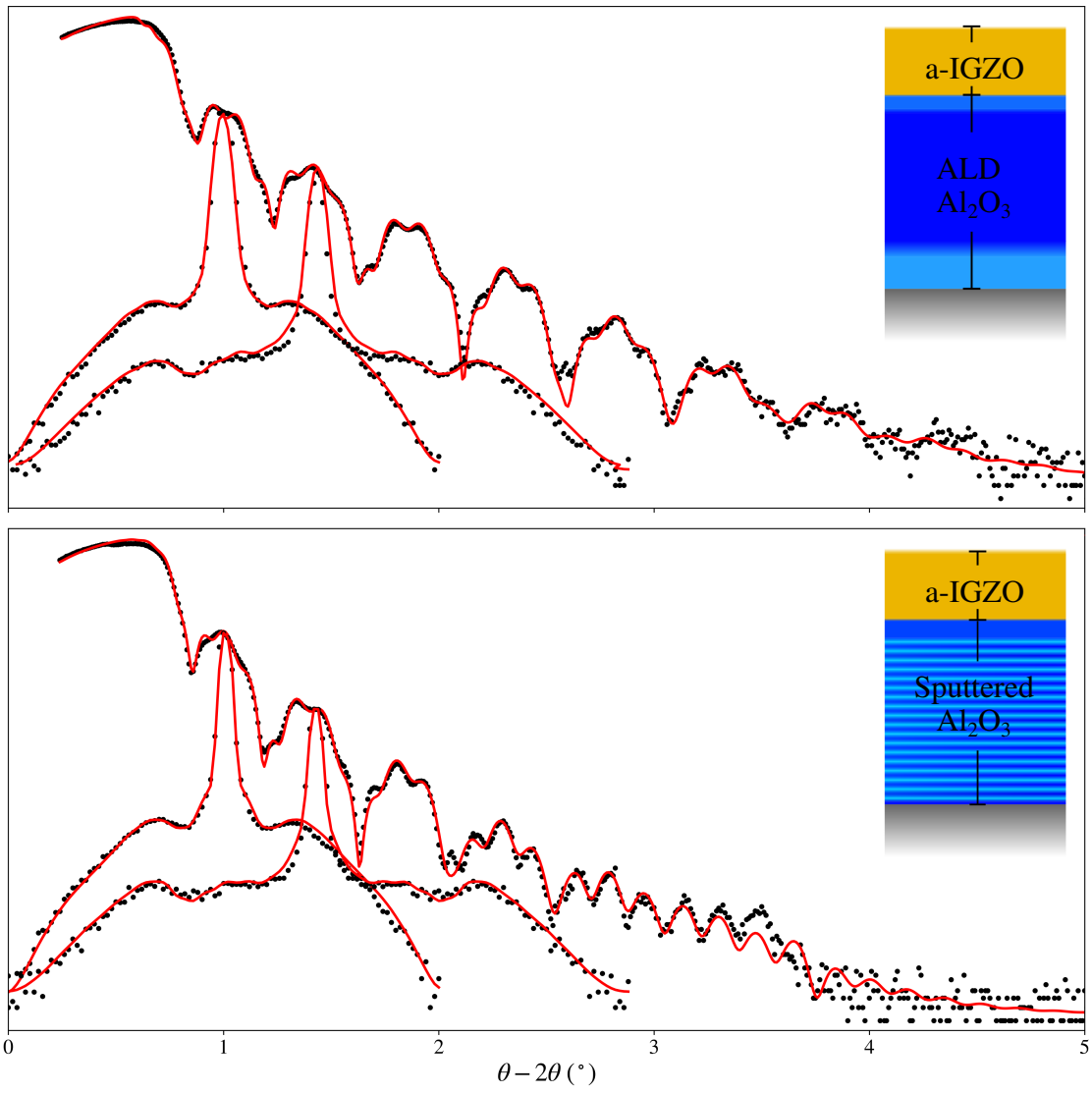


Figure 9.2: Specular XRR data (black dots) with best fitting models (red lines) for ALD and sputter deposited buffer material with 20 nm a-IGZO on top. Theta rocking curves are projected onto the same axis for illustration. The models are simultaneously fitted to both the specular data and the rocking curves.

deposition of a-IGZO, with striking similarity of the thickness and density of the a-IGZO. This work has, however, shown a difference in the structure of the interface itself, with both buffer materials having around 0.5 nm of topological roughness (just over the size of a single aluminium atom), but only the sputtered material shows noticeable chemical intermixing. This is attributed here to a non-stoichiometric Al_2O_3 surface deposited during sputtering that intermixes with the incident a-IGZO. In turn, this intermixing may act to pacify defects at this interface, thereby creating the superior electrical characteristics of TFTs with this buffer layer discussed in chapter 7 [271].

In order to further investigate this, it would be beneficial to perform atomically sensitive chemical analysis of the interface between both buffer layer materials, for example using time-of-flight-SIMS (TOF-SIMS) or transmission electron microscopy (TEM) based analysis, as well as attempting to induce intermixing in the ALD Al_2O_3/a-IGZO interface before fabricating full devices.

9.2 Interface between a-IGZO and Al_2O_3 gate dielectric by Atomic Layer Deposition with annealing

In this section the interface between the semiconducting a-IGZO and the gate dielectric, ALD deposited Al_2O_3, is considered. This interface is of particular importance to device performance as it is home to many of the defects which affect the semiconductor performance, as discussed in section 3.4. The analysis here is similar to that of the buffer layer / a-IGZO interface, in that specular XRR was used to examine the stack structure as a whole before rocking curves were included to examine the detailed structure of the interface.

For this 20 nm, of a-IGZO was sputtered directly onto the standard single crystal silicon with native oxide, under the same conditions as previously. Following this a 50 nm thick layer of Al_2O_3 was deposited by ALD, also under the same conditions as before. However, unlike the investigation of the buffer layer, in which ALD and sputter deposited materials were compared, here only the ALD material was considered, as ALD is the preferred route for this deposition step due to the previously reported improved performance achieved with ALD dielectrics [499–501]. Instead, the effects of low

temperature thermal annealing in air are also described.

In order to investigate the effects of annealing at temperatures compatible with flexible substrates, the initial large silicon wafer was cleaved into multiple samples. These were annealed in air at temperatures between 150 °C and 300 °C for up to 36 hours.

9.2.1 Effect of annealing on layer structure of a-IGZO/Al_2O_3 stack

An example of the XRR data and best fitting model is shown in figure 9.3. Here the three layer model of Al_2O_3, first put forward in chapter 6 and depicted in the inset schematic, is a better match to the data than the single layer Al_2O_3 model, as seen in both the improved FOM and the visually closer fit of the model to the data. This is particularly true at low angles, where most information concerning the top layer is contained. Similar to previously presented fitting, the agreement between the model and the data is very good, giving a high level of confidence in the extracted structural parameters.

Figures 9.4**a)** and 9.4**b)** show the thickness and density for the Al_2O_3 and a-IGZO layers respectively, extracted from the best fitting XRR models. It can be seen from figure 9.4**b)** that the thickness of the a-IGZO did not change significantly over the course of annealing at any temperature, and that the density was similarly little changed (there is some indication of an increase in density with annealing time, but this is a very weak correlation). It is worth noting here that this is somewhat different to the behaviour seen when a-IGZO was annealed in isolation in chapter 8. This may, in part, be due to the capping layer of dielectric preventing the absorption of oxygen from the atmosphere and may also be due to diffusion of gases, such as hydrogen that may be present in the dielectric, into the a-IGZO.

The Al_2O_3 was also not significantly affected by the annealing process, although, there is some indication of weak densification of the material with annealing, but this falls largely within the error margins indicated. A slightly stronger trend is seen in the reduction in thickness of the Al_2O_3 is seen from 6 hours to 36 hours of annealing, which may be due to the removal of residual gases from the deposition process (such as hydrogen, nitrogen, and organic species) released to the atmosphere and/or the a-IGZO beneath [52, 502].

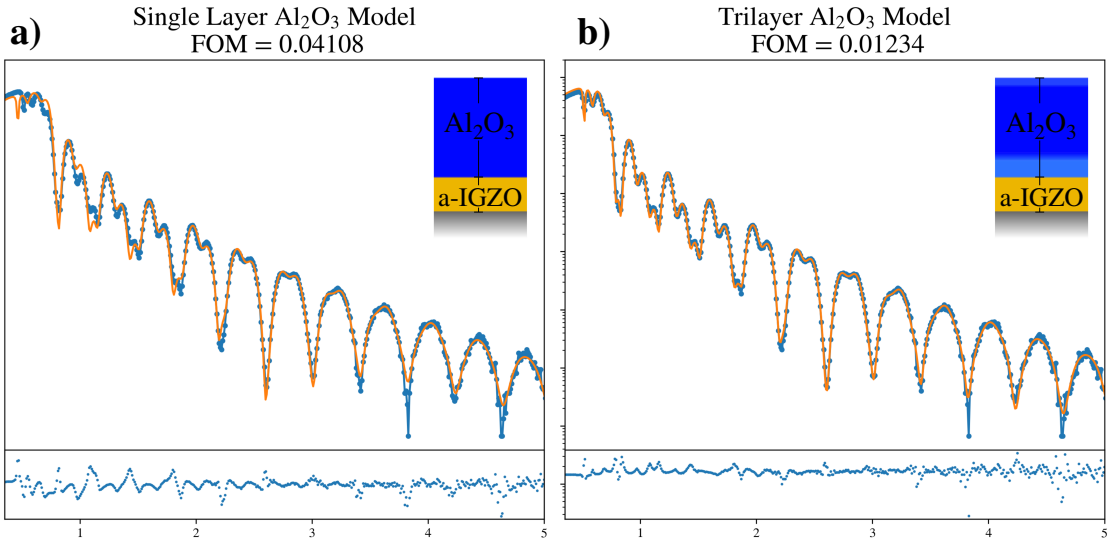


Figure 9.3: Fitting of **a)** a single layer model and **b)** a tri-layer model to the same specular XRR data for an unannealed stack of a-IGZO/Al_2O_3. Better fitting is achieved both visually and according to the lower FOM with the tri-layer mode. For this fitting n=5 was used in the FOM. Inset are schematic representations of the two models used.

9.2.2 Effect of annealing on the interface between a-IGZO and Al_2O_3

The final point of interest is the evolution of the interfacial structure with annealing. This was examined by the inclusion of rocking curve measurements, exemplified in figure 9.5. Figure 9.6 shows the contribution to the interface width from topological roughness (diamond markers) and chemical intermixing (triangle markers). As was seen with the ALD buffer layer above, when initially deposited there was negligible chemical intermixing between the layers and around 0.5 nm of topological roughness. Here, however, this was associated with a significantly higher jaggedness parameter, H=0.24, that may be attributed to the thinner a-IGZO layer compared to the thicker buffer layer (preserving more of the initial growth structure), and other factors associated with the a-IGZO sputtering process.

As annealing proceeded, the level of topological roughness appeared decreased by around 0.2 nm, although there is significant variability in the data here. At the same time, chemical intermixing, particularly at higher temperatures, was induced. While this effect is weak (only 0.14 nm of intermixing is achieved after 36 hours annealing at 300 °C), there is evidence from literature that intermixing at the gate dielectric interface acts to reduce defects and thereby improve performance [271].

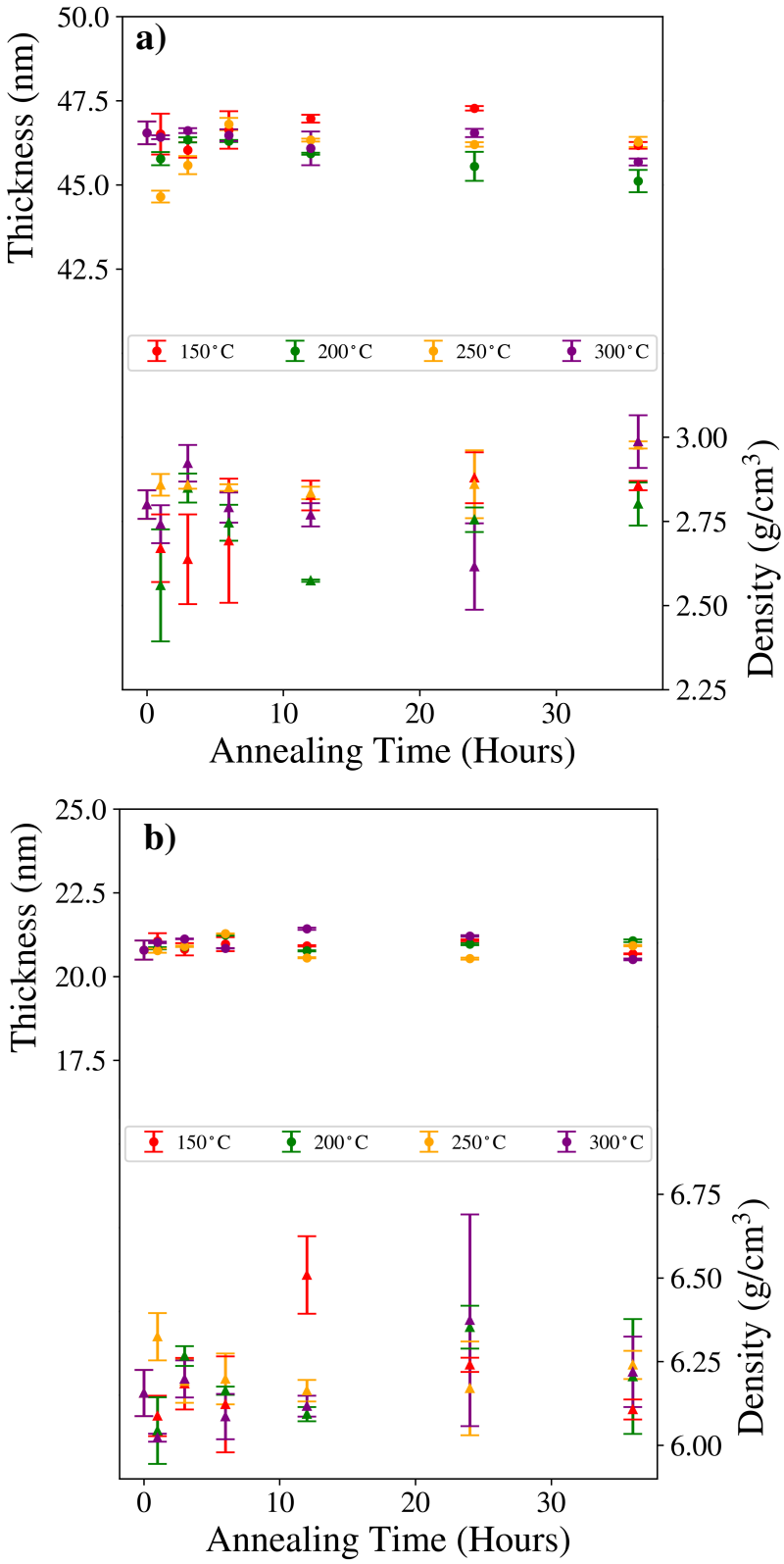


Figure 9.4: Thickness and density of **a)** Al_2O_3 and **b)** a-IGZO in a Al_2O_3/a-IGZO stack, annealed between 150 °C and 300 °C for up to 36 hours in air, extracted from best fitting models of specular XRR data. For comparison the thicknesses and densities in each figure are shown on the same scale.

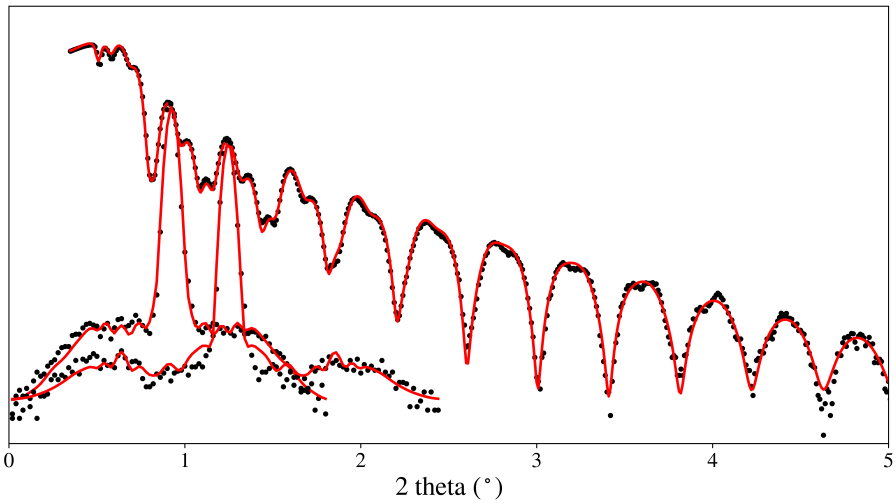


Figure 9.5: Measured data (black dots) and fitted model (red lines) for specular XRR and rocking curves taken for an unannealed stack of a-IGZO/Al_2O_3. The rocking curves are projected onto the 2 theta axis.

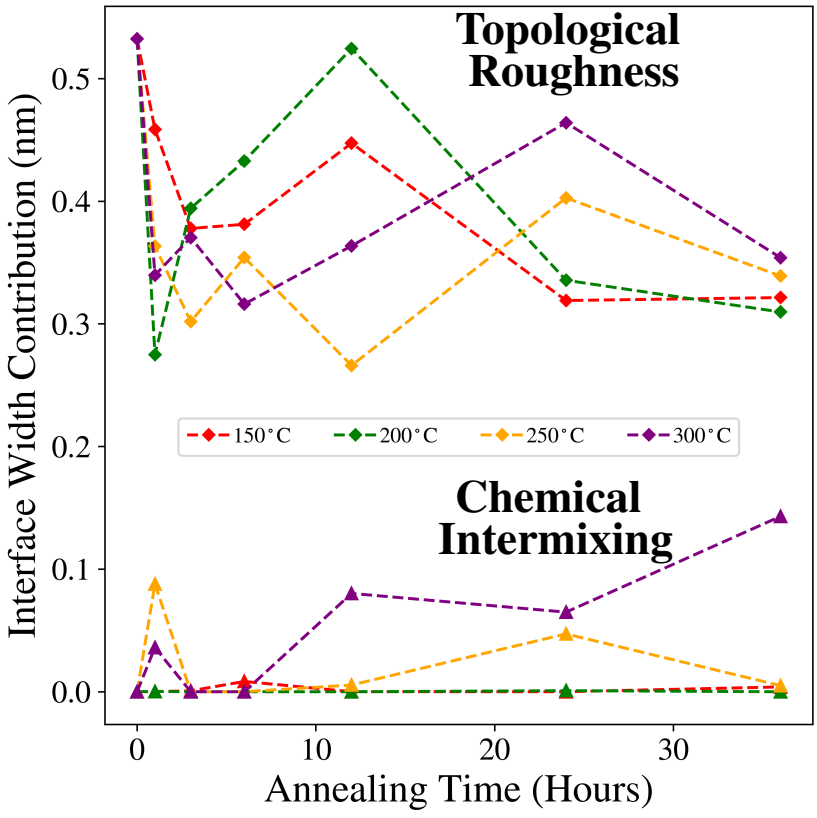


Figure 9.6: Intermixing (triangle markers) and roughness (diamond markers) contributions to the interface width at the interface between Al_2O_3 and a-IGZO, extracted from best fitting simulations of specular and rocking curve XRR data.

9.2.3 Conclusions on annealing of the a-IGZO/Al_2O_3 stack

In this investigation it was found that annealing at low temperatures for up to 36 hours had little measurable effect on the layers within the a-IGZO/Al_2O_3 stack. However, it was found that there is a reduction in the topological roughness at the interface, which has been associated with improved device performance elsewhere [503, 504]. In addition, annealing at higher temperatures, particularly 300 °C, causes some level of chemical intermixing at the interface, and this has also been shown to improve device performance [271], and may have some relevence to the work on improving the performance of the ALD buffer layer. It would therefore be expected that such annealing of devices made with this semiconductor/dielectric stack, would lead to improved device performance through both mechanisms. While such devices were not tested here, this would be the ideal next step.

9.3 Conclusions

The interface between a-IGZO and Al_2O_3, at both the back and front semiconductor channels, has been examined.

In the comparison between Al_2O_3 deposited by ALD and sputtering it was found that the growth of a-IGZO on top of the buffer is not noticeably affected by the deposition method of the buffer material. Some difference between the density of the buffer layers was found, with the the ALD deposited material around 25% more dense than the sputtered equivalent (ρ=3.1 g cm^{-3} for sputtered Al_2O_3 and ρ=3.9 g cm^{-3} for ALD Al_2O_3). However, this does not seem to be the cause of the difference in electrical behaviour seen in devices with such buffers, as it is the ALD material that performs badly in electrical testing. However, there is evidence that the interface between the sputtered buffer and the a-IGZO has comparatively increased levels of chemical intermixing, which has been associated with enhanced device performance due to a reduction of the defect density at this interface. It is therefore possible that such intermixing at the back channel interface also reduces defect density, and so improves device performance.

While the observed intermixing may have some effect on device performance,

particularly with regards to device stability, it is unlikely that this is the only contributing factor causing the degraded device performance seen with ALD buffer material. As the inferior device performance is most significantly characterised by devices which are fully conductive (i.e. do not show any switching behaviour within the range tested), it is possible that the cause is chemical. This is most likely the inclusion of an excess of hydrogen as discussed in section 3.4.1.3, which can cause conductive devices [210]. In order to investigate this further, chemical analysis sensitive to near atomic precision is recommended at this interface. This involves techniques such as TOF-SIMS or the use of EELS or EDX within a transmission electron microscope, or preferably a combination of these. In addition, given the industrial preference for an ALD deposited buffer layer as discussed in chapter 7, the introduction of intermixing at the interface between the ALD buffer and the a-IGZO should be investigated. This may be achieved through chemical roughing of the ALD layer, ion bombardment of a thin seed layer of a-IGZO on top of the buffer before the deposition of the majority of the a-IGZO, or potentially thermal annealing.

In the study of the a-IGZO/dielectric interface, rather than compare different deposition methods for the Al_2O_3, the effect of low temperature thermal annealing was studied with ALD Al_2O_3. Here it was found that annealing had little effect on either the a-IGZO or the Al_2O_3 themselves, but that there was evidence for changes at the interface. These changes included a small reduction in topological roughness for all annealing temperatures and an increase in chemical intermixing at higher annealing temperatures.

Similar to the suggestion for the buffer layer interface, the use of atomically spatially resolved chemical analysis would be beneficial here to accurately capture this evolution. In addition, implementation of this high time/temperature anneal in devices should be tested to investigate whether the improvements expected based on published works are seen.

Chapter 10

Conclusions

In this thesis work was presented looking at three critical layers in thin film transistors based on the metal oxide semiconductor amorphous Indium Gallium Zinc Oxide (a-IGZO), and the interfaces between them, in materials systems developed for electronic applications on flexible substrates. The three layers considered were the a-IGZO layer itself, a buffer layer underneath the semiconductor, and the gate dielectric on top of it, both of which were Al_2O_3. The focus of this work has been examining these layers using X-ray reflectivity (XRR), along with some other techniques, and correlating observed changes with changes in electrical characteristics, with the aim of developing a better understanding of the structure in relation to device performance. The main conclusions drawn from this work are summarised below along with suggestions for future work.

10.1 Conclusions

The first results of this work were presented in chapter 6, in which a systematic study was undertaken to find optimal conditions for the atomic layer deposition (ALD) of aluminium oxide, Al_2O_3, for use as a high dielectric constant field-effect transistor gate insulator. Al_2O_3 was selected as a gate dielectric due to its relatively high dielectric constant (κ $\sim$9) and the large band gap (E_G $\sim$8 eV) making it a good insulator, as discussed in chapter 3.

Before optimising this process it was noted that Al_2O_3 deposited by ALD produced material that was best described as consisting of three distinct layers for the purposes

of fitting the X-ray reflectivity (XRR) data. This trilayer structure was attributed to differences in the behaviour of the Al_2O_3 material in contact with the substrate, with the air, and forming the "bulk" of the layer.

Initially the ALD deposition process was optimised for the pulse and purge times (the time to introduce the precursors, and the time to clear the chamber with the carrier gas between precursor pulses) of the reactant and carrier gases, with recommendations made for optimal times that balance sufficient time for complete layer deposition with the desire to keep these times as short as possible so as to maximise throughput. Recommended pulse times were on the order of 250 ms, while recommend purge times were approximately an order of magnitude longer than this.

As well as optimising the times for this system, this work presents a robust analysis methodology for optimising any new ALD process, which is necessary as the ALD process is very sensitive to changes in the system. Following optimisation of pulse and purge times, several substrate temperatures were examined to ensure the ALD process was carried out within the ALD *process window* described in chapter 4. It was found that at 200 °C the growth rate and the density of the material was maximised, indicating that this is an appropriate temperature for the ALD process to produce optimal material throughput and performance characteristics.

Finally, post-deposition annealing was performed to determine what, if any, effect this process had on the properties of the atomic layer deposited Al_2O_3. This showed that annealing at temperatures that are compatible with flexible polymer substrates (up to 300 °C) had little measurable effect on the materials structural properties.

In chapter 7 an in-depth comparative study of Al_2O_3 used as a buffer layer deposited by ALD and by reactive sputtering, was made. As was explained in the preceding chapter, the material layers deposited by ALD showed a trilayer structure. However, in comparison it was found that the material deposited by sputtering also showed non-homogeneous characteristics, but with a somewhat more complex structure. A comparison of several different models showed that the sputtered Al_2O_3 layer had a structure best described as comprising of a series of around 20 sublayers. These sublayers are attributed to variations in the deposition associated with the movement of the sample during the sputter deposition process.

Before comparing the ALD and sputter deposited materials, it was noted that significant variation in device performance was dependent upon the day of the week on which the buffer layer was deposited. Significant degradation of the device characteristics was observed for material deposited on a Friday compared to the following Monday. This was correlated with an enhanced variation in the density of the sublayers on the Friday, and has been postulated to be linked with increased levels of contamination within the sputtering system that was evidenced by an elevated base pressure within the system. Subsequently it was recommended, on the basis of this work, that the system is more thoroughly evacuated before deposition proceeds, allowing a lower base pressure to be achieved, corresponding to a lower level of contamination, and that this be kept constant throughout the week.

Following this, comparison of the physical properties and surface energies of the ALD and sputtered Al_2O_3 was made in an attempt to explain why TFTs fabricated with an ALD Al_2O_3 underlayer consistently failed to show functional switching behaviour. Analysis here showed that the physical parameters, in particular the density and surface roughness of the materials, suggest that the ALD material should be of superior quality to the sputtered material in terms of expected device performance. However, it was also shown that the surface energy of the two materials, particularly when exposed to treatments mirroring the full TFT production process, was strikingly similar ($\sim$1% variation). As this comparison does not give a compelling explanation of the difference in device performance, further study was suggested, some of which was performed and detailed in chapter 9, and some of which is discussed below.

The semiconducting a-IGZO layer was considered in chapter 8, in particular the effect of thermal annealing over a range of temperatures and times compatible with flexible substrates was systematically studied. It was found that annealing had a significant impact on material density, and that this impact was dependent both on the temperature and time of the annealing . It was also observed that, unlike Al_2O_3, a-IGZO did not show any significant sub-structuring within the layer and thus the material can be treated as homogeneous.

The changes in density of the layer were interpreted as being due to two competing mechanisms; the structural relaxation of the amorphous phase, and the absorption of

oxygen by the material. This was represented in a model by a linear combination of two exponential functions, representing these mechanisms. Both of these mechanisms were considered to be thermally activated processes, dependent on both time and temperature, with differing energy barrier heights. Average energy barriers for structural relaxation and oxygen absorption were found to be 531 meV and 1423 meV respectively, extracted from fitting an Arrhenius-type equation to the characteristic times for each process. This chapter also showed that by optimising the annealing process, through the systematic study presented, significant improvements in device characteristics were achieved.

The final chapter of results is a detailed study of the interface between the a-IGZO semiconducting layer and the other two insulating layers already discussed. The buffer layer to a-IGZO and the gate dielectric to a-IGZO interfaces were discussed in turn, using similar XRR analysis as in previous chapters and also included measurements of the transverse diffuse X-ray scatter in order to separate the topological roughness and chemical intermixing that define these interfaces. The sublayer structuring observed previously for both the ALD and sputter deposited Al_2O_3 was also present in these samples, evident in the XRR analysis despite the increased sample complexity introduced by the inclusion of the a-IGZO layer.

Comparison of the ALD and sputtered buffer layers in these samples showed that, similar to the layers in isolation, the density of the ALD material was higher than that of the sputtered material. It was also found that the growth rate and the density of the a-IGZO deposited on these different buffer layers was very similar, indicating negligible difference in the growth mechanics of the a-IGZO. There was, however, evidence that the interface between the sputtered buffer and the a-IGZO had comparatively higher levels of chemical intermixing, which has been associated with enhanced device performance when seen at the dielectric to a-IGZO interface due to a reduction of the defect density at this interface. It is therefore possible that such intermixing at the back channel interface also reduces the defect density, and so improves device performance.

The impact of thermal annealing on the interface between the dielectric Al_2O_3 and the a-IGZO was examined through another systematic study over a range of temperatures and times. It was observed that annealing had little effect on the structure of either the a-IGZO or the Al_2O_3 layers, but there was evidence of changes at the interface.

These changes included a small reduction in topological roughness for all annealing temperatures and an increase in chemical intermixing at higher annealing temperatures. Again, it is suggested that such intermixing may be beneficial to device performance.

Taken as a whole, this work shows some consistent themes which may inform future research and development work.

The persistent presence of sublayer structuring in both forms of Al_2O_3 examined suggests that this material is very sensitive to changes in processing. In particular this is made clear in the discussion in chapter 7 of the impact of day of the week on material structure and subsequent device performance. Two key points should be taken from this. In order to improve device performance over the long term, optimisation of the deposition processes is critical. Arguably a more important point, at least from a commercial point of view, is about the consistency of device characteristics. In order to be able to design circuits based on the the transistors considered here, consistency of the transfer characteristics is key, both consistency between devices made in the same batch and from batch to batch for devices made using the same process. The only way to achieve such consistency is to strictly control the conditions during fabrication, minimising and understanding variation between runs.

This work also makes clear the importance of the need for detailed studies of the material properties and in particular the systematic study of influencing factors. This was particularly true in chapter 8, in which a systematic study of annealing of a-IGZO led to a significant improvement in device characteristics.

This work also demonstrates that the interfaces between layers, particularly the interfaces with a-IGZO, are of particular importance. This is due to the interfaces being the primary area in which current flow occurs, and so the structure of the interfaces is of great importance. In order to develop improved devices, the understanding of these interfaces must be further developed and this understanding leveraged to improve device performance, as suggested below.

10.2 Future Work

There are several areas in which the work presented here could be extended, particularly through the use of additional techniques and further *in vivo* characterisation of materials in fully processed devices.

The optimisation of the ALD process presented in chapter 6 was performed by characterising the physical parameters of the deposited films. In order to better characterise this process *in situ*, measurements of the ALD material could be performed, for example using ellipsometry or infrared spectroscopy, as described by by Langereis et al. [411, 505]. Using such measurements, the optimised pulse and purge times could be ascertained using fewer depositions, reducing both the cost and the time to develop the process. In addition, the introduction of additional high-κ gate dielectrics would be of significant interest, for example TiO_2, as a multilayer stack with Al_2O_3, combining the large bandgap of the Al_2O_3 with the very high κ of TiO_2 [506].

The comparison of ALD and sputtered buffer layers, both in isolation and in conjunction with a-IGZO, showed only very small differences, which are unlikely to account for the observed difference in device performance. In order to further investigate this issue, it is suggested that detailed chemical analysis of both the materials themselves and the interface between the buffer and the a-IGZO is performed. This may take the form of thermal desorption spectroscopy (TDS) to examine trapped gaseous species and impurities; Secondary Ion Mass Spectroscopy (SIMS) or X-ray Photoelectron Spectroscopy (XPS) to examine layer stoichiometry and the atomic bonding environments; Scanning Tunnelling Microscopy (STM) to probe local electrostatic environments, and Time of Flight SIMS (TOF-SIMS) to examine the chemical structure across the interface.

In addition, work that aims to replicate the intermixing seen at the interface with the sputtered buffer with an ALD buffer should be undertaken to establish if this does in fact contribute to the superior performance. This could be achieved through chemical roughing of the ALD layer; ion bombardment of a thin seed layer of a-IGZO on top of the buffer before the deposition of the majority of the a-IGZO; or potentially thermal annealing.

Similarly, increasing the level of intermixing at the dielectric interface, either through the thermal annealing presented in chapter 9 or one of the routes described above, should be trialled in full TFT devices in order to see if this reduces the density of trap sites at the interface.

Finally, further investigation of the optimal stoichiometry of the a-IGZO is warranted, particularly with regard to the oxygen content of the layer. It was shown in chapter 8 that the oxygen content of the deposited film was below the stoichiometric value, and it was suggested that oxygen absorption by the layer is one of the mechanisms controlling the change in density of the film. In order to optimise the a-IGZO, a detailed investigation of the effect of systematically varying the oxygen content in the film should be carried out. For this, while chemical analysis of the film would be of great interest, it would be insufficient to optimise for a fully stoichiometric film because, as mentioned in chapter 3, the presence of oxygen vacancies actually dopes the a-IGZO with additional charge carriers and increases device performance. Therefore, a study combining both chemical analysis and fabrication of devices at a variety of oxygen levels is suggested to achieve the best possible performance.

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